SOLUTION PROCESSING OF LOW VOLTAGE, LOW TEMPERATURE, SUSTAINABLE, TRANSPARENT OXIDE FIELD-EFFECT TRANSISTORS

by

Yu Liu

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ABSTRACT

Solution processing is a promising method for manufacturing large-area, low-cost electronic devices. Oxide is a group of earth abundant, environmental friendly materials with tunable energy bands and charge carrier concentration, so they are widely applied as semiconductors, dielectrics, and conductors in flat panel displays, photovoltaics, lighting, sensors, and radio-frequency identification tags (RFIDs). Oxide thin films can be solution processed with good control of stoichiometry and microstructures with proper design of precursor solution, deposition condition, and post-annealing procedures.

In this thesis, oxide dielectric and semiconductor thin films were fabricated and analyzed. Ion incorporation in alumina dielectrics offers exceptionally high capacitance and thus significantly reduces operation voltage of field-effect transistors (FETs). Alumina capacitance can be manipulated by incorporation of alkali metal ions with different bond strength with oxygen, including potassium, sodium, and lithium. Ion-incorporated aluminas capacitors exhibited a strong frequency dependence of capacitance with a possible electric double layer capacitor (EDLC) behavior. To investigate the effect of alkali metal ion on the detailed alumina capacitance and AC conductivity response, the frequency, temperature, and thickness dependences of alumina capacitance were determined. Distinct transistor stability behavior under pulsed gate bias stress observed among ZTO FETs with ion-incorporated aluminas and plain aluminum oxide gate dielectrics. Distinct bias stress induced change in drain current, threshold voltage, and saturation field-effect mobility of ion-incorporated aluminas and plain alumina based FETs reflects different interfacial charge trapping behavior and suggests possible formation of defect states.

Solution processing of semiconductor materials on large area flexible substrates usually involves a trade-off among facile charge transport, high-capacitance/low voltage transistor gates, and low processing temperature. In this research, we fabricated all-oxide field-effect transistors using sol-gel solution processing techniques at 200-250 °C temperatures. A simplified aqueous precursor solution preparation method was discovered to prepare ZnO as semiconducting layer. ZnO FETs with SiO_2 gate dielectric fabricated at 200 °C exhibited a saturation field-effect mobility of 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and a typical on/off current ratio on the order of 10^4. In addition, combustion precursors were synthesized to fabricate a high capacitance sodium ion-incorporated alumina (SA) dielectric with annealing below 250 °C. With the combustion-processed SA gate dielectric, ZnO FETs were fabricated and successfully operated at 5 V.

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DEDICATION

To my beloved Father and Mother

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CHAPTER I

Introduction

1.1 Introduction to field-effect transistors

Ever since the invention of transistors by John Bardeen, Walter Brattain, and William Shockley in 1947, phenomenal progress have been achieving in modern electronics and this makes a revolutionary impact on every aspect of human life. As the cornerstone of modern electronics, transistor works as the fundamental building block of various electronic devices, including computers, television, cell phones, and cameras. A field-effect transistor is a unipolar transistor operated by single type charge carrier conduction, which is modulated by an electric field applied at the gate electrode. In silicon based microelectronics, metal oxide semiconductor field-effect transistor (MOSFET) is the dominant design with conducting channel formation based on minority charge carrier inversion in bulk single crystalline silicon substrate. Over the past decades, the advancement of microelectronics is achieved by miniaturization of transistors' size described by Moore's law. However, in some other applications, flat panel displays for example, large area and low cost are considered as the main criteria in device design and manufacturing, thin film transistor (TFT) emerges as the alternative transistor structure to fulfill the requirements.[1, 2] A thin film transistor is clearly defined as "A field-effect transistor made of nonsingle crystal semiconductor film deposited on an insulating substrate".[2] As its name implies, charge transportation channel forms by major carrier

accumulation, instead of inversion, in a layer of semiconductor thin film in TFTs. The semiconductor thin film can be coated on arbitrary substrates, including glass, plastic, metal, or silicon. Therefore, the fabrication of TFT devices is not restricted by the ingot diameter of single crystalline silicon, expanding its application in low cost, large-area electronics, such as flat panel displays, photovoltaics, sensors, and RFIDs.[3-9]

A typical TFT is composed of a gate dielectric layer, a semiconductor layer, and three electrodes named as source, drain, and gate. Figure 1.1 shows a cross section view of a TFT. Both n and p-type semiconductors can be used as the active layer conducting current by transporting electrons or holes. As mentioned previously, TFT operates in accumulation mode, which means conductive channel cannot be formed in semiconductor layer without applying a gate voltage. As a potential creates between gate and source, dielectric layer polarizes, attracting or repelling charge carriers in semiconductor layer. If a positive (negative) gate voltage applied to gate electrode, electrons (holes) in n-type (p-type) semiconductor active layer will be attracted to the dielectric/semiconductor interface. After reaching a critical charge carrier density, conductive channel forms at the interface. By applying a proper drain voltages, charges can be pumped to drain electrode and turn on the transistor.

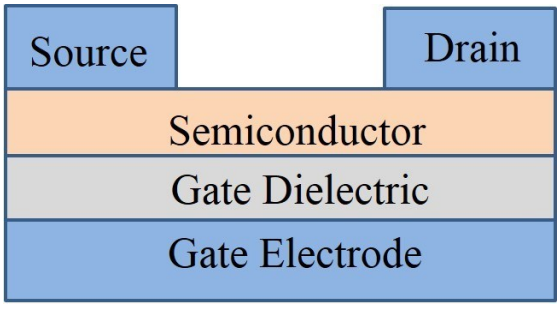


Figure 1.1 Schematic view a bottom gate top contact TFT.

In FETs, drain current (I_D) can be described by two equations related to two operation regions, depending on the value of V_D and V_G. In linear region ($V_D << V_G - V_T$), I_D increases linearly as the increase of V_D and it is calculated by Equation (1.1).[10]

$$I_{D,lin} = \frac{W}{L} \mu_{lin} C_i (V_G - V_T - V_D / 2) V_D \tag{1.1}$$

where $I_{D,lin}$ is the drain current in linear region, W is the channel width, L is the channel length, μ_{lin} is field-effect mobility in linear region, and C_i is dielectric capacitance per unit area.

As V_D increases to a certain value, a saturation behavior of I_D is seen in output characteristics (I_D versus V_D plot). In saturation region ($V_D \geq V_G - V_T$), I_D is expressed by Equation (1.2).

$$I_{D,sat} = \frac{W}{2L} \mu_{sat} C_i (V_G - V_T)^2 \tag{1.2}$$

where $I_{D,sat}$ is the drain current in saturation region, μ_{sat} is field-effect mobility in saturation region.

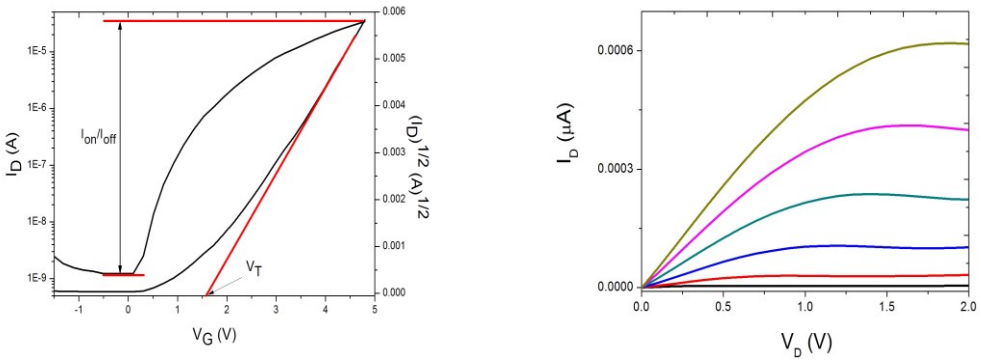
The field-effect mobility is the drift mobility of charge carriers under applied source and drain electric field. Field-effect mobilities extracted from these two regions are not equal, and saturation field-effect mobility is more commonly reported in literature. Field-effect mobility calculated based on FET is a device dependent parameter and need to be distinguished from material mobility, such as Hall mobility.

Threshold voltage is the gate voltage for which the channel conductance (at low drain voltages) is equal to that of the whole semiconducting layer.[11] From transfer characteristic, threshold voltage data was determined by the gate voltage intercept of the linear extrapolation of square root of drain current curve. On/off current ratio (I_{on}/I_{off}) is a parameter represents drain current modulation as applied gate voltage. It is measured by difference between the highest drain current level and lowest current level in the transfer characteristics. Figure 1.2 shows the extraction of threshold voltage and On/off current ratio from transfer characteristics of a transistor. Another important parameter in FET is subthreshold slope (S), which represents the change in gate voltage needed to increase the drain current by a factor of 10.[12] S is expressed by Equation (1.3):

$$S = \frac{dV_G}{d(\log I_D)} = \ln 10 \frac{dV_G}{d(\ln I_D)} \tag{1.3}$$

Subthreshold slope is also a parameter reflects dielectric/semiconductor interface quality as it is related to interface trap density D_{it}, shown in Equation (1.4):

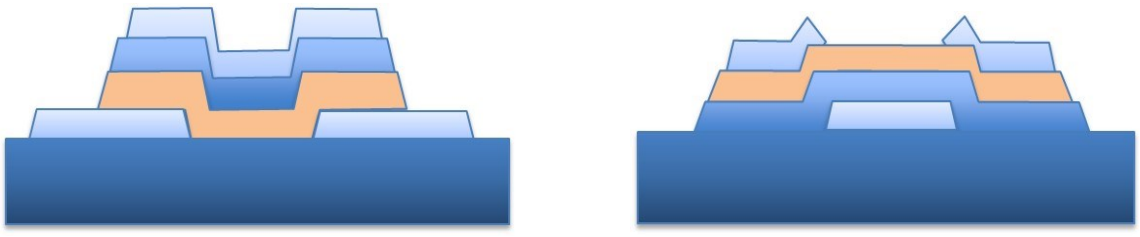
$$D_{it} = [\frac{Sq}{\ln(10)kT} - 1] \cdot \frac{C_i}{q^2} \tag{1.4}$$



(a) (b)

Figure 1.2 (a) Transfer characteristics and (b) output characteristics of a TFT with n-type semiconductor channel layer.

Generally, there are four types of TFT configurations: (a) staggered top gate (STG); (b) staggered bottom gate (SBG); (c) coplanar top gate (CTG); and (d) coplanar bottom gate (CBG), as shown in Figure 1.3.[13] In staggered structures, semiconductor layer separates gate electrode from source and drain electrodes in opposite sides; while in coplanar structures, all three electrodes locate on the same side of the semiconductor layer. Staggered bottom gate is the most commonly used TFT configuration because it achieves high device performance with simple processing steps. Top gate configurations are usually used when the semiconductor material is unstable in air.



(a) (b)

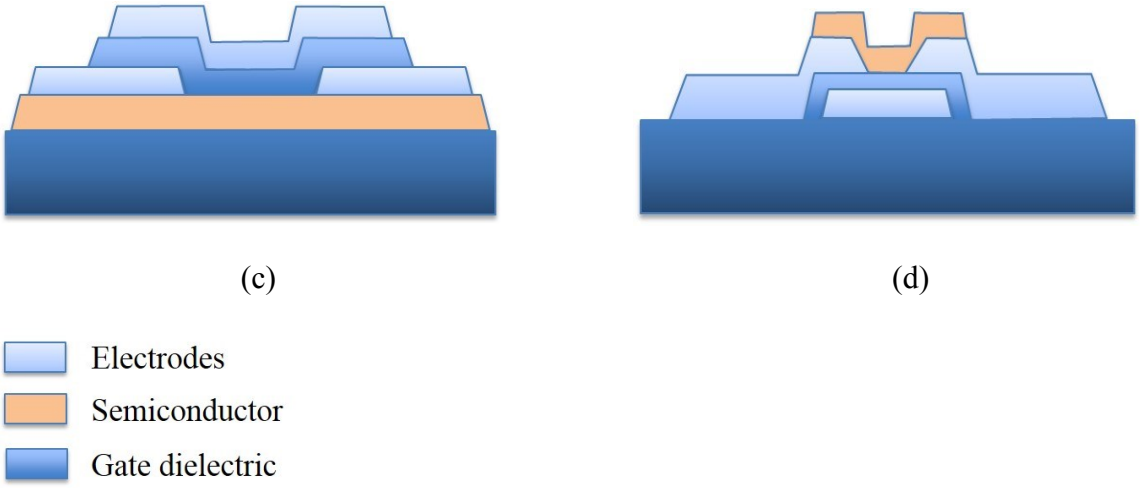


Figure 1.3 Typical TFT configurations (a) staggered top gate (STG); (b) staggered bottom gate (SBG); (c) coplanar top gate (CTG); and (d) coplanar bottom gate (CBG).

1.2 Introduction to high-k dielectrics

Depending on application, various types of inorganic, organic and hybrid materials are used as gate dielectric in TFTs. SiO_2 is a benchmark gate dielectric material which can be easily grown by thermal oxidation on silicon substrate. It has high thermal and chemical stability, high crystallization temperature (1100 °C), wide band gap (8.9 eV), and low defect density – all of these merits make SiO_2 as the dominant gate dielectric material in microelectronics for several decades. As the miniaturization of feature size, SiO_2 dielectric thickness decreases to increase the gate capacitance. When SiO_2 thickness decreases to less than 2 nm, drastic leakage current is generated by tunneling through thin SiO_2 layer and this increases power consumption and reduces device stability.

To keep up with the trend of miniaturization described by Moore's law, high-k dielectric materials replaced SiO_2 as the gate dielectric. In 2007, HfO_2, a high-k dielectric with relative dielectric constant of 25, was used as the gate dielectric in Intel's 45 nm Core 2

quad core processor for the first time. In large-area macroelectronics application, high-k dielectrics also play an important role in reducing energy consumption of electronic devices and maintain a high device performance. Aside from oxide dielectrics, some other types of dielectric materials are proved to be able to achieve high capacitance in field-effect transistor applications. These materials includes (a) ion-gel dielectrics; (b) hybrid self-assembled multilayer nanodielectrics; (c) self-assembled monolayer (SAM)-treated inorganic dielectrics; (d) anodized metal dielectrics, (e) nanostructured and nanocomposite dielectrics; and (f) solid electrolyte dielectrics.[14-24]

Unite area capacitance of a capacitor is given by Equation (1.3):

$$C_i = \frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{1.3}$$

where C_i is dielectric capacitance per unit area, C is capacitance, A is area of electrode, ε_0 is vacuum permittivity ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), ε_r is relative dielectric constant of the dielectric, and d is dielectric thickness.

According to this equation, unite area capacitance of a capacitor is proportional to relative dielectric constant of the dielectric and it is inversely proportional to dielectric thickness. With high-k dielectrics, a high capacitance can be maintained even though the dielectric thickness decreases. Dielectric properties of high-k dielectric materials and silicon based dielectrics are shown in Table 1.1 and Figure 1.4.[25]

Table 1.1 Dielectric constant (K), experimental band gap and CB offset on Si of gate dielectrics.

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8 (not ALD)
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8

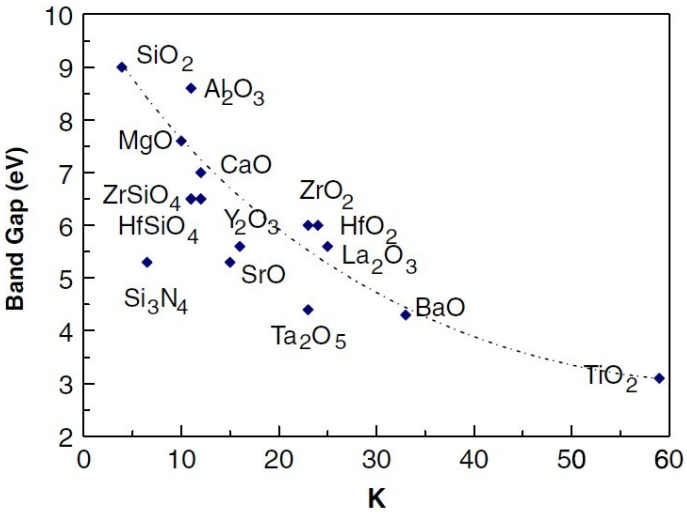


Figure 1.4 Band gap versus dielectric constant plot of common dielectric materials.

1.3 Introduction to amorphous oxide semiconductor

In large-area electronics application, high semiconductor mobility is not the most critical design parameter and single-crystal silicon is not the dominant semiconductor material. Polycrystalline and amorphous silicon semiconductor, oxide semiconductors, and organic semiconductors are the most popular options in large-area electronics application. The study of transparent conductive oxides (TCOs) dates back to sixty years ago. In 1954, In_2O_3:Sn (ITO) was reported as the first TCO material, followed by SnO_2 and ZnO.[26] For a long period of time, TCOs were widely used as transparent window electrodes and interconnects. Only since a decade ago, oxide material was used in active applications, designated by the invention of amorphous oxide semiconductors (AOS) semiconductors TFTs in 2004.[27]

Amorphous oxide semiconductors are a group of ionic oxides composed of post transition metal cations with an electronic configuration $(n\text{-}l)d^{10}ns^0$ ($n \geq 4$). Distinct from conventional amorphous silicon and amorphous chalcogenides, AOS maintain high mobility in the amorphous state due to their unique band structure. In silicon, the valence band and conduction band are formed by highly directional sp^3 orbitals. In single crystalline silicon, very high charge carrier mobility (>1000 cm^2/Vs) is attributed to large overlap of sp^3 orbitals and large conduction band dispersion in the periodic single crystal structure. However, in amorphous silicon (α-Si:H), the small overlap of sp^3 orbitals is unfavorable for conduction band dispersion and thus limits the mobility to less than 1 cm^2/Vs. In ionic oxides, valence band is composed of occupied O 2p antibonding bands and conduction band is composed of unoccupied cations bonding band.[28-31] The conduction band of ionic oxides is primarily composed of s orbitals of cations. With a principle

quantum number n≥4, the spatial spread of neighboring s orbitals are very large, and thus resulting in a small effective mass of electrons in these oxides. Due to the spherical symmetry of s orbitals, the spatial spread of orbitals is not affected by the variation of bond angle in the amorphous state and high mobility is achieved in amorphous post transition metal oxide semiconductors.

Figure 1.5 lists 15 post transition metal elements with $(n-l)d^{10}ns^0$ (n≥4) configuration.[4] Among them, Ag, Au, and Ge are expensive metals. Cd, Hg, Tl, Pb, and As are excluded from AOS application due to their high toxicity. Cu is used in p-type semiconductor. In the remaining six elements, Zn, Ga, In, Sn are the most commonly used in AOS. The application of Sb and Bi as AOS has not been reported yet. Indium gallium zinc oxide (IGZO, In:Ga:Zn=1.1:1.1:0.9, atomic ratio) is the first commercialized AOS as active layer in AMLCD application. In AOS, In incorporation increases the electron concentration. Ga is introduced to suppress oxygen vacancy formation due to its stronger chemical bonds with oxygen compared with Zn and In. In this way, carrier concentration can be tuned at a low level ($< 10^{16}$ cm^{-3}) to achieve a low off current and large on/off current ratio.[4, 27] Indium-based amorphous oxides, including IGZO and IZO, exhibit good electrical properties even with low temperature processing. However, it would be problematic for indium-based oxides in large-area electronics application due to the high cost and potential shortage of indium. Zn and Sn are abundant, inexpensive, and nontoxic, so they considered as ideal choices in AOS application. Both ZnO and SnO_2 are wide band-gap n-type semiconductor materials. ZnO has a direct band-gap of 3.37 eV and possess three crystal structures: wurtzite, zincblend, and rocksalt.[32-34] Among them, wurtzite is the most stable structure at ambient conditions. SnO_2 has a rutile crystal structure and has direct band-gap

of 3.63 eV.[35] In ZTO, a competition of ZnO wurtzite crystal structure and SnO_2 rutile structure formation inhibits crystallization and thus remains at amorphous states for low temperature processed ZTO. ZTO is also an n-type semiconductor with a direct band-gap of 3.3 ~ 3.9 eV. The wide band-gap range is due to Burstein-Moss shift and variation of ZTO composition and structure. ZTO has very high thermal and chemical stability, especially a high acid resistance. ZTO also has a high resistance to scratching and very low surface roughness.[36, 37] Solution processing of ZTO FETs was first reported in 2007 with a metal chloride based precursor solution.[38] In this study, ZTO thin films were deposited by spin-coating method followed by post-annealing at 600 °C for 1 hour in air. The annealed films are very uniform and smooth with an amorphous structure. FETs fabricated by spin-coating ZTO thin film on heavily doped p-type silicon substrate with 100 nm SiO_2. Operating at 40 V, ZTO FETs exhibited a field-effect mobility of 16 cm^2/Vs, an on/off current ratio of 10^5, and a threshold voltage of 2 V.

11	12	13	14	15	
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.92	4
47 Ag 107.87	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	5
79 Au 196.97	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.98	6

Figure 1.5 Post transition metal elements with $(n-l)d^{10}ns^0(n\geq4)$ configuration.

1.4 Processing of thin film materials and devices

Thin films are fabricated by a variety of deposition techniques. Three major types of thin film deposition methods are: physical vapor deposition (PVD), chemical vapor deposition (CVD), and solution processing. Physical vapor deposition is carried out in high vacuum chamber by depositing vaporized source materials onto the surface of substrate. Typical PVD methods used for industrial and research purposes includes magnetron sputtering, electron beam/thermal evaporation, pulsed laser deposition (PLD), and molecular beam epitaxy (MBE). Magnetron sputtering is currently the most popular technique for thin film deposition because it grows high quality thin films and it is capable for large area thin film growth. In magnetron sputtering, ionized Ar bombards the surface of target material and knock out atoms from the target to substrate.

In chemical vapor deposition, volatile precursor molecules decompose in activated environment (high temperature or plasms) and deposit onto heated substrate. Atomic layer deposition (ALD), metalorganic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), and low pressure chemical vapor deposition (LPCVD) are examples of the common chemical vapor deposition methods.

1.5 Solution processing of oxide thin film materials and devices

Solution processing of thin films is extensively pursued recently in large-area electronics, owing to its simplicity, low cost, high through-put, and complex composition materials deposition capability.[39] In solution processing, inexpensive precursors are used and deposition usually occurs in atmosphere without using high vacuum chamber and high

energy source. In printing processing, for example, precursors are directly deposited onto the substrate and this can significantly reduce the waste of raw materials. Compared with PVD, solution processing also significant increases the variability of materials to be coated. For instance, hybrid thin films with organic and inorganic composite can be fabricated by solution processing. In this case advanced material properties and functionality would be able to be realized. Common solution processing techniques used for oxide thin film growth include spin-coating, dip-coating, drop-casting, inkject printing, spray-coating, screen printing, chemical bath deposition, doctor blade coating, aerosol jet, etc.[40]

Sol-gel solution processing is a typical solution processing method which involves the transformation of molecular precursor into oxide network. Sol-gel processing of thin films includes three steps, shown in Figure 1.6: (1) precursor solution preparation, (2) thin film deposition, and (3) heat treatment of as deposited film. In sol-gel processing, metal alkoxides, metal salts, metal acetates, or metal acetylacetonates are dissolved in organic solvents or aqueous solutions. The preparation of precursor involves a series of steps including hydrolysis, polymerization, condensation, nucleation, and growth.[41] In sol-gel process, two routes are widely used: (1) alkoxide precursor in organic solvents and (2) inorganic salts in aqueous solutions. Hydrolysis steps of alkoxides precusor is expressed as:

$$M-OR+H_2O \rightarrow M-OH+ROH$$

and condensation:

$$M-OH+RO-M \rightarrow M-O-M+ROH \quad \text{or}$$

$$M-OH+HO-M \rightarrow M-O-M+H_2O$$

Typically, transition metal precursors have high reaction rate of hydrolysis and condensation, which makes it difficult to control the morphology and structure of the oxides. Chelating ligands including carboxylic acids, alkanolamines, alkylamines, β-diketones, and peroxo complexes are often used as stabilizers in organic and aqueous sol-gel precursor solutions to prevent uncontrolled precipitation of metal hydroxides by modifying the reactivity of the precursors with increased coordination number of the metal ions.[41-43] For the preparation of zinc oxide, aluminum oxide and related materials, inorganic salts, like nitrates and chlorides, or organic salts, such as acetates and acetylacetonates, are dissolved in alcoholic solvent. After vigorous stirring after a period of time, alkoxide or alkoxy-complexes form in the solution and then transform to metal-oxygen network by polymerization. After film coating, post-annealing is a key process for achieving ideal materials structure and properties. Annealing temperature, time, and gas atmosphere significantly affect precursor decomposition and defect generation in solution processed materials.

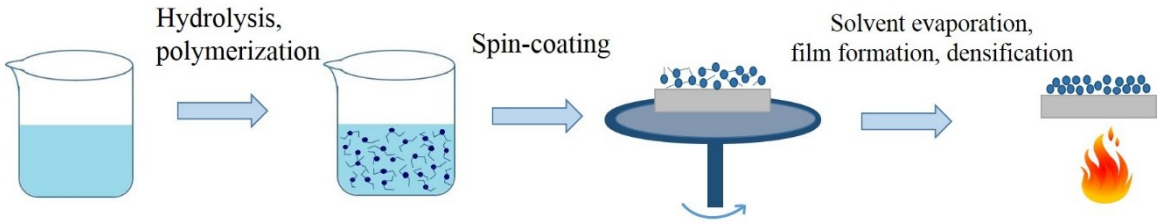


Figure 1.6 Sol-gel solution processing steps.

1.6 Outline of thesis

In Chapter 2, we will discuss the effect of sodium ions incorporation on the structure, dielectric behavior of sodium-incorporated aluminas and compare the performance ZTO FETs with sodium-incorporated alumina and plain alumina gate dielectrics. Besides, the device stability and transistor encapsulation issues will also be addressed.

Chapter 3 gives a detailed comparison of dielectric behavior of aluminas with the incorporation of different alkali metal ions (K^+, Na^+, Li^+) as well as plain alumina without ion-incorporation. With the observation of distinct capacitance and AC conductivity behavior among these dielectrics, an electric double layer capacitor model with alkali metal polarization near the alumina/Al electrode interface is proposed to explain the high capacitance observe in ion-incorporated aluminas at low frequencies. Different frequency dependent capacitance and AC conductivity behavior observed in ion-incorporated aluminas was attributed to the variation in alkali metal ions polarizability in alumina matrix related to metal to oxygen bond strength.

Alkali metal ion polarization in alumina is significantly affected by pulsed gate bias stress and we will introduce this in Chapter 4. ZTO FETs with PA, SA, LA, and Al_2O_3 gate dielectric showed distinct transfer characteristics under pulsed gate bias stress with a pulse width of 1 ms and period of 5 ms, 10 ms, and 50 ms in the gate bias stress duration of 730 seconds. Careful analysis of threshold voltage shift, capacitance and saturation mobility decrease as applied pulsed gate bias stress was carried out to suggest different interface charge trapping levels and new defect formation behavior in ion-incorporated aluminas.

In Chapter 5, we will introduce two types of sol-gel precursors for low temperature fabrication of all oxide FETs. A simplified aqueous precursor solution preparation method was discovered to prepare ZnO and ZTO as semiconducting layer. ZnO field-effect transistors (FETs) with SiO_2 gate dielectric fabricated at 200 °C exhibited a saturation field-effect mobility of 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and a typical on/off current ratio on the order of 10^4. In addition, combustion precursors were synthesized to fabricate a high capacitance sodium ion-incorporated alumina (SA) dielectric with annealing below 250 °C. With the combustion-processed SA gate dielectric, ZnO FETs were fabricated and successfully operated at 5 V.

CHAPTER II

Effect of sodium ion in alumina dielectric properties

2.1 Introduction

High performance, large-area solution-processable field-effect transistor (FET)-based circuits are key components in the application of printable, low-cost electronics, such as large-area, inexpensive, low-voltage, and transparent sensors.[1–13] With conventional organic and oxide semiconductor semiconductors, a high gate voltage, for example >30V, has to be applied to these devices (e.g. if using 100nm SiO_2 as gate) to drive usable source-drain currents, which significantly limits the development of commercial components from these semiconductor materials. According to the saturation-regime drain current equation of FETs, operating voltage and input power could be reduced by increasing either saturation field-effect mobility of semiconductors or the capacitance of gate dielectrics. The latter option is more and more feasible as abundant high-k and thin film dielectric materials have become available. Extensive research on high-k dielectrics has been carried out in the application of both traditional Si-based FETs and novel solution processed flexible FETs.[14–19]

In microelectronics, there has been a drive to scale down transistor size for faster logic operation and increased computing power. Simply shrinking SiO_2 dielectric thickness leads to a surge in leakage current due to quantum tunneling effects. A high-k material allows the gate film to achieve a desired high capacitance with larger thickness. Thicker films can help reduce the leakage current arising from structural defects and carrier tunneling.

However, some high-k materials are unsuitable for gate layers in FETs[14] because of one or more of the following: (1) formation of polycrystalline films rather than glasses. Crystallization will give rise to grain boundaries at which leakage current is concentrated. One of the advantages of the SiO_2 gate is that it maintains at an amorphous state up to 1100 °C. Many high-k oxides have low crystallization temperature which prevents them from being used as gate materials.[20] The candidate to replace SiO_2 in silicon technology, HfO_2, has crystallization temperature above 900 °C. (2) Insufficient band offset with semiconductor layers. A small band gap offset will result in leakage current by charge injection and give rise to hot-carrier emission. SiO_2 has a band gap as large as 8.9 eV. (3) Thermal and chemical instability in the presence of the semiconductor layer, for example leading to oxidation or diffusion phenomena. (4) Surface defects leading to operational instability of FETs. One advantage of SiO_2 is the small defect density due to its high process temperature, and covalent bonds with low coordination which allow any dangling bonds to self-heal back to the network. In contrast, many other ionic bonding oxides such as Al_2O_3, HfO_2, and ZrO_2 have higher defect concentrations.

Exceptionally high capacitance was discovered in alumina dielectric thin film by incorporating proper amount of sodium ions a couple of years ago by our group.[21] The sol-gel derived thin film (75nm) possesses a dielectric constant (k) up to 170, which is much higher than traditionally used SiO_2, with k = 3.9, and other possible alternatives to SiO_2, such as ZrO_2, k = 23, and HfO_2, k = 20. The zinc tin oxide (ZTO) FETs made by using this sodium incorporated alumina gate layer can output hundreds of microamperes with an operational voltage of 2V, a significantly lower voltage than the same ZTO device using SiO_2 as gate layers (30V for 100nm SiO_2).

A typical sodium incorporated alumina (SA) materials is sodium beta-alumina (SBA). SBA has a layered crystal structure in which loosely bonded sodium ions are sandwiched by two spinel blocks made of Al and O atoms, so in the ab plane the sodium ions can move easily giving a good electrical conductivity.[22] However, in the c direction, the movement of sodium ions is confined by the spinel blocks. SBA attracts much attention due to its high ionic conductivity, of great of importance for solid-state electrolytes. In gate dielectric application, the fast movement of sodium ions in alumina matrix provides additional ionic polarization in alumina and thus significantly increase capacitance.

Using aforementioned criteria to review SA, we found that (1) SA is a moderate glass former. The SA materials we study here have nominal bulk crystallization temperatures of 720 ^{o}C and 830 ^{o}C based on powder samples. (2) The band gap is large; SA along the c axis has a band gap of 8.8 eV, comparable to 8.9 eV of SiO_2, and much larger than other oxide gate material candidates, such as HfO_2, band gap 5.6 eV, ZrO_2, band gap 4.7-5.7 eV. (3) SA has good chemical stability in the presence of popular semiconductor oxides such as indium tin oxide and zinc tin oxide up to 600 ^{o}C based on our experiments. (4) The chemistry of SA allows routes to possible defect passivation, though intrinsically it shares the defect challenges of other oxide dielectrics.

In this chapter, we will have detailed discussion about the degree of crystallinity of solution processed SA thin films and the role that sodium ions play in achieving high capacitance of SA dielectric. Besides, possible side effects, such as increase of leakage current, threshold voltage shift, caused by sodium ion diffusion will be covered.

2.2 Experimental section

Sodium incorporated alumina and plain alumina sol-gel solutions are made based on Yoldas's paper.[23] For SA, sodium acetate (0.041 g) was dissolved in 50 ml water and heated to 90 °C. $Al(OC_4H_9)_3$ (1.41 ml) was heated at 90°C with vigorous stirring. The sodium acetate solution (for SA) at 90 °C was added, and the temperature was increased to 95°C with stirring for 0.5 h to form AlO(OH) precipitates. 5ml of dilute mixed acid (0.2N HNO_3 and 0.2N HCl, 1:1 ratio) was used for peptization. The sol was kept under continuous stirring at 95 °C for 0.5 h and then heated further to 110 °C to boil off water. With 10ml water removal, the sol approached the gel point. The clear gel was then filtered through a syringe filter (0.45μm) and coated over ITO-coated glass (Corning Boro-Aluminosilicate Glass with 30nm ITO coating supplied by Delta Technologies Limited, part number CB-90IN-1,105). This process was repeated three times. This gel-derived glass layer was heated starting from 350 °C, ramping the temperature to 830 °C. When the temperature of the furnace reached 830 °C, it was immediately turned off. Once the furnace cooled down to 600 °C, the samples were removed.

A solution-processed transparent ZTO semiconductor could be solution-deposited over SA or alumina-coated ITO glass substrates: $ZnCl_2$ (0.05 M) and $SnCl_2$ (0.05 M) were dissolved in 25 ml 2-methoxyethanol solvent with ultrasonication. The substrate was dip-coated with this solution at 2mm/s with an angle 60° to the horizontal and immediately placed on a 75 °C hot plate. This process was repeated four times. The coated substrate was inserted into a preheated 600 °C furnace and kept for 15 min to form a thin layer of continuous polycrystalline ZTO, 60 nm thick as confirmed by SEM.

An alternative way to coat SA on ITO glass is to use spin coating. 4.68 g $Al(NO_3)_3 \cdot 9H_2O$ and 0.11g sodium bisulfate (for SA) with 11:1 molar ratio are dissolved into 25ml methoxyethanol. The same number of moles of acetylacetone as Al ions is added into the solution as stabilizer and the mixed solution is kept under stirring for 6 h. The solution is filtered through a 0.45 μm PTFE filter and spin coated on the cleaned ITO glass. First, the solution is spin coated at low speed (500 rpm) for 6 seconds and then the spin speed is accelerated to 3000 rpm within 3 seconds and kept at 3000 rpm for 30 s. One time spin coating results in a film thickness of 41 nm, measured by profilometer. The coated glass goes through the same annealing process as the dip-coating method. Then the whole process is repeated once to achieve desired thickness about 80 nm. ZTO film also can be spin coated onto this SA or alumina layer. 0.3 M ZTO solution for spin coating can be made by mixing $Zn(O_2CCH_3)_2 \cdot 2H_2O$ and $SnCl_2$ at 1:1 ratio in methoxyethanol with acetylacetone having the same concentration as the total of the Zn and Sn ion concentrations. Aluminum electrodes (100nm thick) were deposited in a vacuum evaporator using a slim-bar transmission electron microscopy grid (200 mesh) as a shadow mask.

Transistor performance of SA and Al_2O_3 based ZTO FETs was characterized by Agilent 4155C semiconductor analyzer. Capacitance of SA and Al_2O_3 thin films was measured with a metal-insulator-metal structure by The Agilent 4284 precision LCR meter. LCR meter measures the impedance of the sample and then calculates capacitance based on the phase angle. A phase angle of -90^o means the device is a complete capacitor (current is all capacitive). When the phase angle deviates from the -90^o, this means that the device not only has a capacitance component but also has a conductance component. The capacitance

measurement at lower frequency between 20Hz and 1000Hz is not as accurate as at higher frequency because the phase angle is farther from -90^{o}. The typical phase angle at frequency from 20Hz to 1000Hz is -75^{o} and above that frequency range the phase angle is about -85^{o}. Therefore, we report capacitance data here from 1kHz to 1MHz.

A Dimension 3100 Atomic Force Microscope (AFM) (Bruker Nano, Santa Barbara, CA) was used for the measurements. The contact mode images were obtained using Si_3N_4 contact mode tips (Model DNP) with a nominal spring constant of 0.12 N/m. A scan rate of 2 Hz was used to obtain images (2 x 2) μm to (10x10) μm. Root-mean-square (RMS) values were obtained from a (2x2) μm scan. The average value of multiple RMS measurements is reported. The high resolution transmission electron mictroscopy (HRTEM) picture was taken by a Philips CM 300 FEG TEM (field emission gun operating at 297 kV). The X-ray diffraction, using the configuration typical for grazing incidence small-angle X-ray scattering (GISAXS), was carried out at Beamline X13B at the National Synchrotron Light Source at Brookhaven National Laboratories. The Aluminum electrodes of the transistor devices (100 nm thick) were deposited in a vacuum evaporator using a slim-bar transmission electron microscopy grid (200 mesh) as a shadow mask. The width and length of the channel are about 100 μm and 10 μm respectively.

2.3 Crystal structure of SA thin film

Crystallinity of SA thin film was first characterized by x-ray diffraction. No diffraction peak was observed in both dip-coated and spin-coated SA thin films annealed at 830 °C. To have a better understanding about crystal structure of SA films, focused ion beam (FIB)

was used to cut a 50 nm thin slice of the SA film for TEM observation. Figure 2.1 shows the cross section of the SA layer on top of ITO layer. Because indium and tin are much heavier elements than Al, the ITO film is shown in the dark region and SA in the bright region. Clear lattice fringes from the ITO region indicates crystallization of the film; however, the whole SA region only shows an amorphous state morphology. Additionally, grazing incidence XRD was carried out to confirm the amorphous structure of SA film. The GIXRD pattern is shown in Figure 2.2. The rings in the GIXRD pattern correspond to polycrystalline materials. After calculating the crystal plane distance, the d spacings are 4.26Å, 3.04Å, 2.62Å, 2.49Å, 2.23Å, 2.07Å, 1.847 Å which all correspond to ITO but not SA.

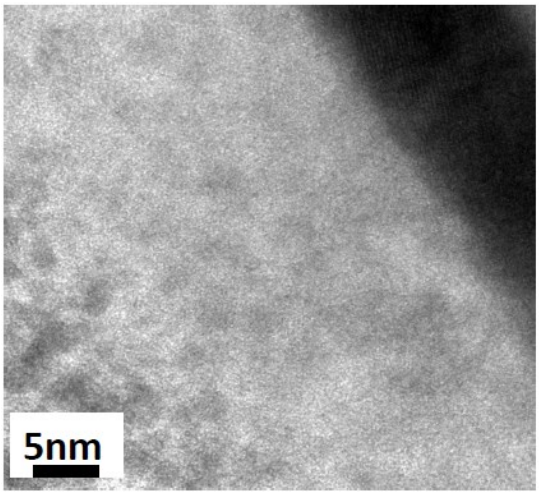


Figure 2.1 High resolution transmission electron microscopy image of SA/ITO interface.

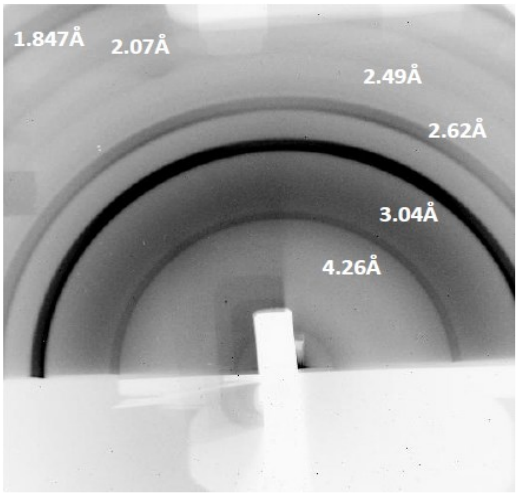


Figure 2.2 Grazing incidence X-ray diffraction pattern of SA coated on ITO glass.

When the annealing temperature increased to 1000 ºC and annealing time increased to 15 hours, the 90nm thin film is clearly crystallized. Because of the low softening temperature (850 ºC) of ITO glass that we used for devices, we instead used a Si wafer with 300nm thick SiO_2 layer as the substrate. The XRD pattern of the crystallized thin film is shown in Figure 2.3. Main peaks in the pattern correspond to (102), (107), (108), (206), planes of the SBA crystal structure.[24] This result suggests that layered spinel beta-alumina crystal structure can be identified in SA thin film at high temperature with a long annealing time. With an annealing temperature less than 1000 ºC, short-range order would form in SA thin film and partially formation of layered alumina crystal structure would provide space for sodium ion polarization. The hump in the XRD pattern is from the amorphous state SiO_2 on the Si wafer substrate.

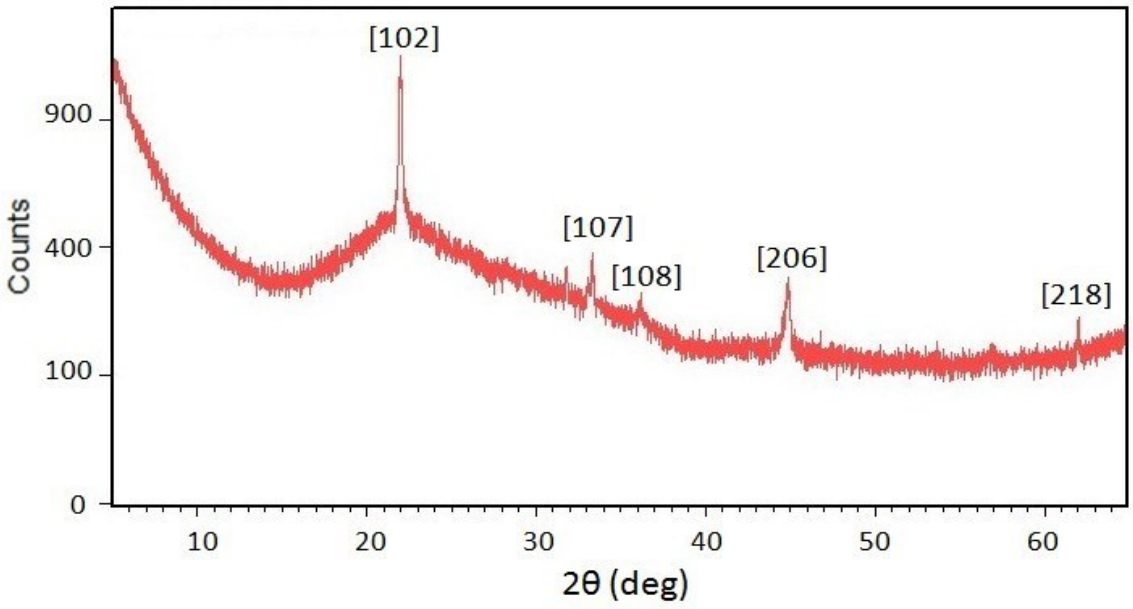
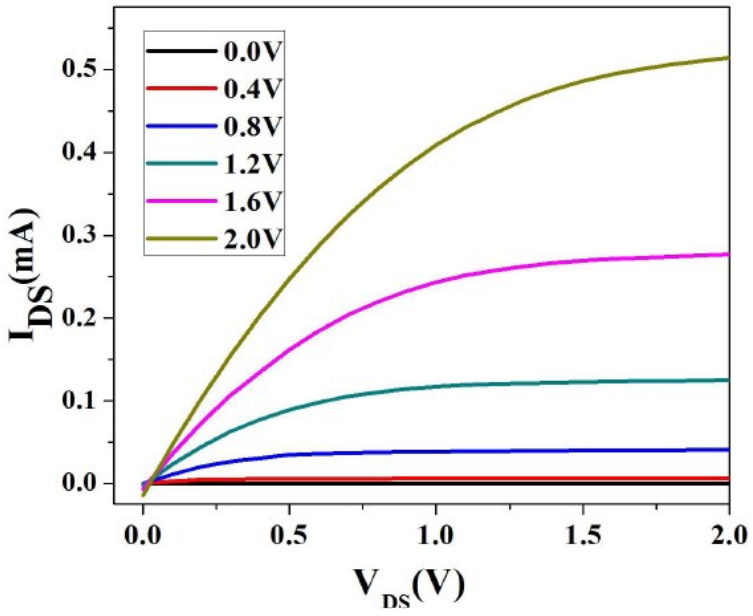


Figure 2.3 XRD pattern of SA film prepared by spin-coating with annealing at 1000 ºC for 15 hours.

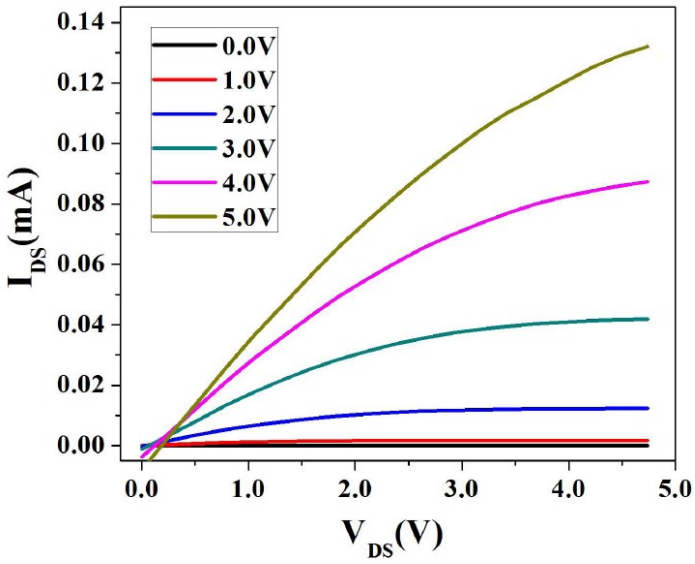
2.4 Comparison between Al_2O_3 and SA as gate dielectrics

As a high-k material, alumina is a popular choice as gate dielectric in FETs applications.[25-27] However, in most cases, alumina film was fabricated by atomic layer deposition method, and of course, the resulting film lacks sodium ions. Herein, a parallel study of the solution processed SA and plain alumina film was performed to determine the role of sodium ion in the dielectric properties of SA. SA and Al_2O_3 thin film with similar thickness (Al_2O_3 is 90nm thick and SA is about 80nm thick) was coated as the gate materials on ITO coated Corning glass substrate. ZTO semiconductor active layer and aluminum source and drain electrodes were then deposited on top to form a bottom gate top contact TFT.

From the output curve shown in Figure 2.4, ZTO FET with Al_2O_3 gate dielectric operated at 5V demonstrated a maximum output current around 0.11 mA, while the ZTO FET with SA gate dielectric operated at 2V showed an 4 to 5 times larger output current compared with Al_2O_3 FET. The ability of SA to reduce operational voltage is evidently demonstrated. SA based ZTO FET showed a higher field driven mobility value, 18cm^2/Vs, than Al_2O_3 based ZTO FET, 10cm^2/Vs. The on/off ratios of the two devices are both on the order of magnitude of 10^4. Since we use the same dip-coating technique to fabricate the ZTO layer on both SA and alumina, the difference in FET performance would be caused by the different dielectric layers and dielectric/semiconductor interface.



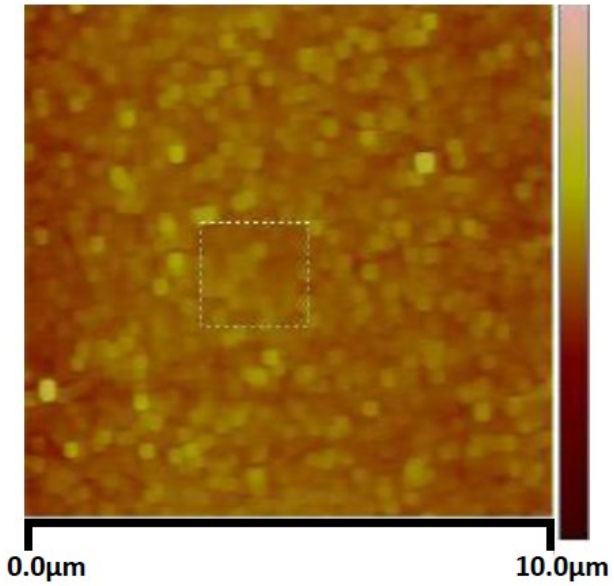
(a)



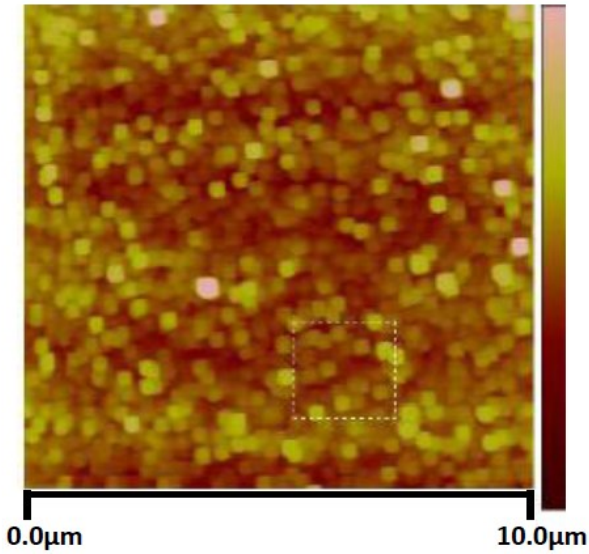
(b)

Figure 2.4 Output characteristics of (a) ZTO FET with SA gate dielectric and (b) ZTO FET with Al_2O_3 gate dielectric.

AFM images shown in Figure 2.5 indicate that SA has lower roughness than Al_2O_3 film. The RMS roughness of SA film is 1.15 nm and that of Al_2O_3 film is 1.65 nm. We suggest that the roughness difference can be a factor in the mobility difference between the two types of devices. A possible reason for Al_2O_3 having higher roughness is that Al_2O_3 is easier to be crystallized than SA. And consequently SA has a rougher surface than SA when annealed at the same temperature. SA bulk sample has a crystallization temperature higher than 720 °C[24] However, the γ phase and δ phase of Al_2O_3 start to crystallize at 380°C and 520 °C.[28] From this perspective, the SA is better glass former than Al_2O_3 in terms of surface roughness, a conclusion that was not anticipated in our earlier work.



(a)



(b)

Figure 2.5 AFM picture of (a) SA and (b) Al_2O_3 thin film. The squared-off feature edges are an artifact of the scanning direction.

One concern for SA as gate dielectric was that as an ionic conductor, sodium ions could move through the alumina matrix causing large gate leakage current. Based on our observations, SA based ZTO FET devices did not show higher leakage current than Al_2O_3 based ZTO FET. The small leakage in SA films is more likely caused by structural defects such as pinholes in the film, rather than sodium ion motion. This I_g that we do observe is quite stable and does not show a trend of diminishing under operation. If the leakage current is caused by sodium ions diffusion, leakage current diminishing at long operational time as the depletion of sodium ions should be observed. We thus conclude that leakage current is mainly electronic, not ionic.

2.5 Frequency-dependent capacitance of SA thin film

Comparing SA and Al_2O_3, different dielectric properties is caused by the additional sodium ion polarization in SA thin film. AC capacitance of SA and Al_2O_3 thin film with similar thickness was measured at different frequencies, showing in Figure 2.6. SA showed a much higher capacitance at lower frequency and decreased to a value similar to Al_2O_3 samples at high frequency; while Al_2O_3 displayed a very small frequency dependence. We tried three different annealing temperatures, 300 °C, 500 °C and 700 °C, for SA thin films, keeping the annealing time at 1h. SA capacitance is also depends on annealing temperature. Capacitance of SA thin films annealed at 300 °C, 500 °C, and 700 °C is shown in Figure 2.6. The capacitance of 300 °C annealed samples is lower than 500 °C and 700 °C annealed samples over the entire frequency range, but the difference diminished with increasing frequency. The annealing temperature dependence of SA capacitance can be explained by two reasons. First, high annealing temperature is favorable for complete removal of

undesired organic residual in solution processed SA film and thus forms a more intact SA film structure. Moreover, while GIXRD and TEM indicated no long-range order, it is possible that high annealing temperature facilitates the formation of short-range order in SA film, leading to a more regular nanocrystalline alumina structure which is favorable for sodium ion polarization.

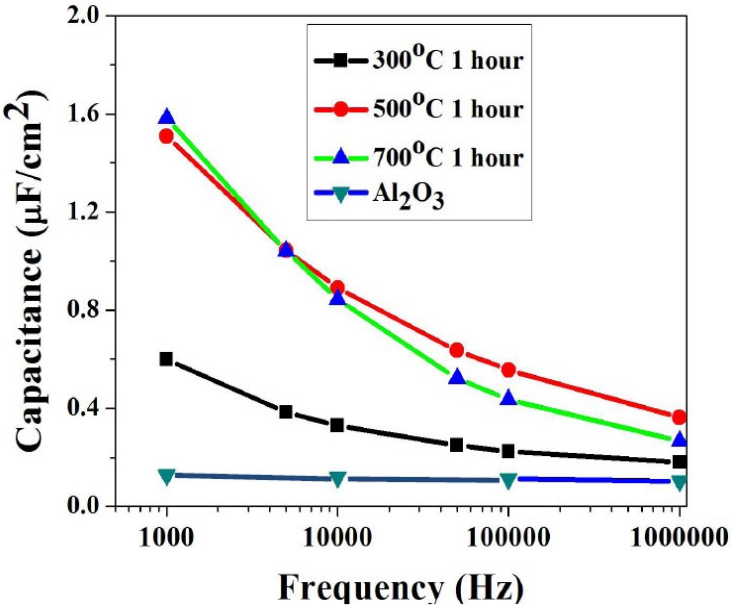


Figure 2.6 Frequency-dependent capacitance of SA and Al_2O_3 thin films annealed at different temperatures.

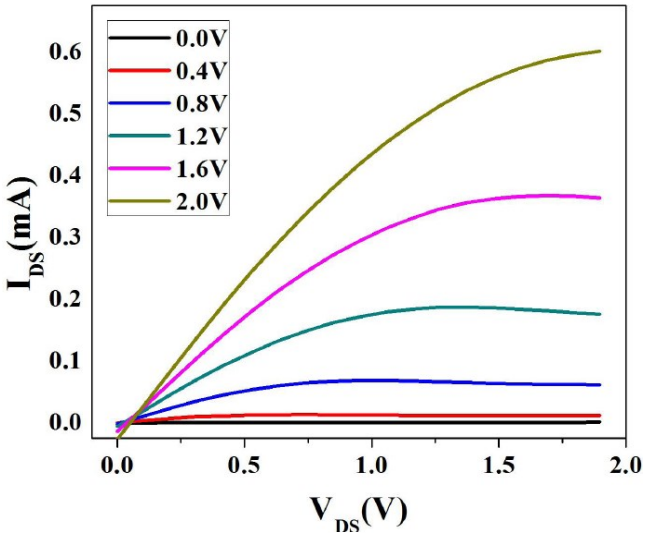
2.6 X-ray photoelectron spectroscopy (XPS) analysis of sodium ion polarization

Another experiment to investigate the polarization behavior of sodium ions in SA film is carried out by measuring the near-surface sodium atom concentration for SA film before and after bias voltage by XPS. A copper foil was pressed onto SA film on ITO glass as a top electrode. 2V bias was applied on SA film for 30 minutes. After applying bias voltage,

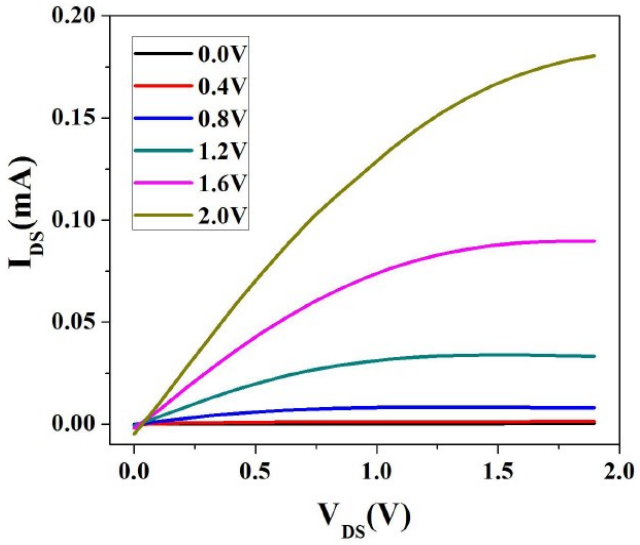
the atomic concentration of SA film was characterized by XPS. SA film without applying bias voltage was also measured by XPS as a control sample. The detected sodium atom concentration of the bias voltage applied sample showed a three times higher sodium atom concentration (atomic ratio Na/Al=1.2/28.2) than the control sample (atomic ratio Na/Al=0.4/28.3). Here, the increased sodium atom concentration reflects the part of polarized sodium ions by bias voltage which remains to be trapped at the surface after the removal of bias. After removing the bias, it is possible that some sodium ions could have relaxed back to their original position. This experiment is a direct observation of sodium ions movement in SA film under bias voltage.

2.7 Device stability issues in ambient environment

Despite the promising properties we have noted for SA based ZTO FETs, the performance degrades in the ambient condition. Typically, within 24 hours, the output current could drop by a factor of three, as shown in Figure 2.7. The device degradation could be because of at least two atmospheric components. It is well known that amorphous oxide semiconductors (AOS), such as ZTO and IZO are sensitive to water, oxygen and even vapors of common solvents such as ethanol and acetone.[29] Physically absorbed O_2 is electrically neutral, but if the O atoms became chemically bonded with defects in AOS, the O becoming negatively charged will deplete the conduction band. Water, on the other hand, acts like a donor to generate more free negative carriers. The moisture sensitivity of SA was reported previously.[30] Physisorbed water in SA can increase the conductivity of the sodium ions. As sodium ions become more mobile, the interface charge accumulation could become more significant, causing the degradation of the field driven current.



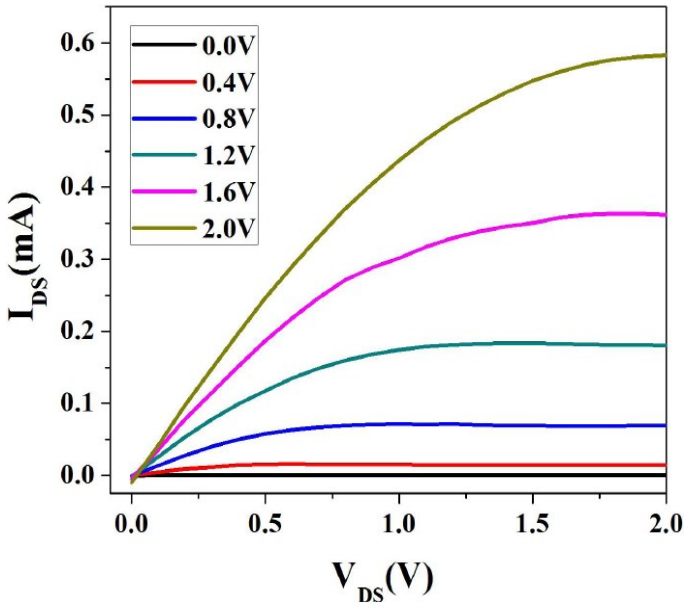
(a)



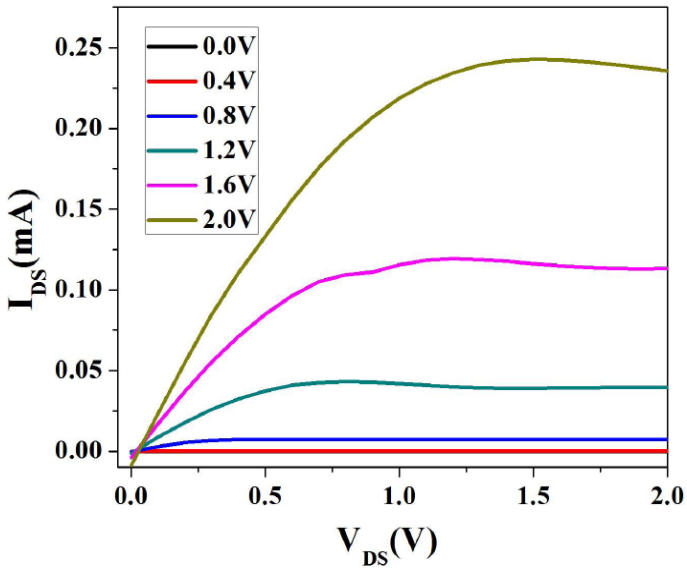
(b)

Figure 2.7 Output characteristics of (a) fresh ZTO FET with SA gate dielectric and (b) ZTO FET with SA gate dielectric stored in ambient condition for 24 hrs.

We found that the SA based ZTO FETs stored under vacuum show a much better device stability with no degradation in 72 hours. This result suggests that the device degradation could be prevented by encapsulation. We considered one particular candidate material, Cytop, for encapsulation. Cytop is an amorphous fluoropolymer with high hydrophobicity. As coating layer, it has excellent transparency, electrical insulation, chemical resistance and moisture resistance. Cytop was spin-coated at 5000 rpm for 30 seconds on the top of as fabricated FET, followed by heat treatment on hotplate at 90 °C for 5 minutes. A slowed degradation was found after coating Cytop. As shown in Figure 2.8, after 24 hours, there is no obvious decrease of the current. After 72 hours, drain current decreased to about one third of the original current, which is about the same amount as the current decrease in unencapsulated device after 24 hours.



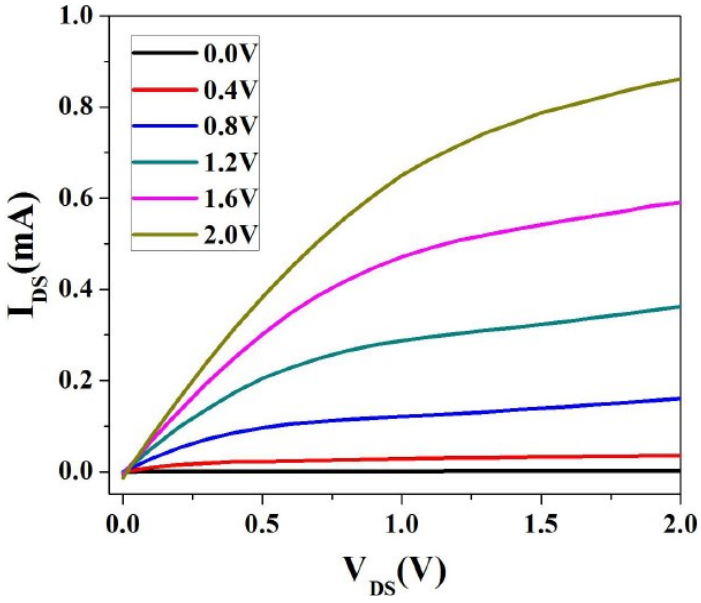
(a)



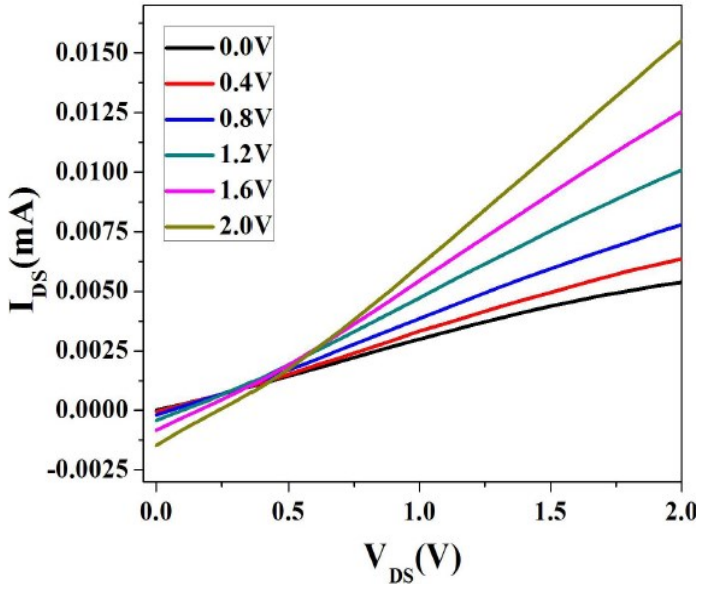
(b)

Figure 2.8 Output characteristics of ZTO FET with SA gate dielectric encapsulated with Cytop stored in ambient environment for (a) 24 hrs and (b) 72 hrs.

Hexamethyldisilazane ($(CH_3)_3SiNHSi(CH_3)_3$) (HMDS) was also coated as an encapsulation layer to increase the top surface hydrophobicity of the transistor. However, HMDS would have a chemical reaction with ZTO layer. As shown in Figure 2.9, the output curve changed significantly including both magnitude of the output current and threshold voltage, implying a strong doping effect arising from the reaction between ZTO and HMDS. Judging from the shape of the output curve, the device after HMDS treatment has threshold voltage shifted significantly in the negative direction, indicating that the HMDS could act as a donor to the ZTO. This experiment indicates that ZTO could potentially be used in sensors for amines.



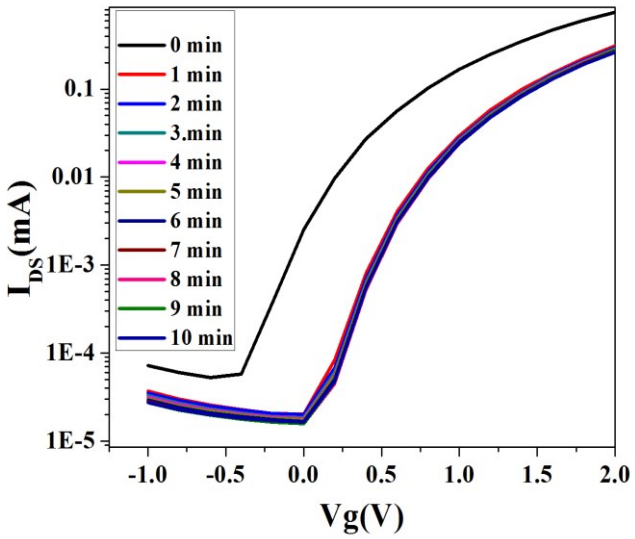
(a)



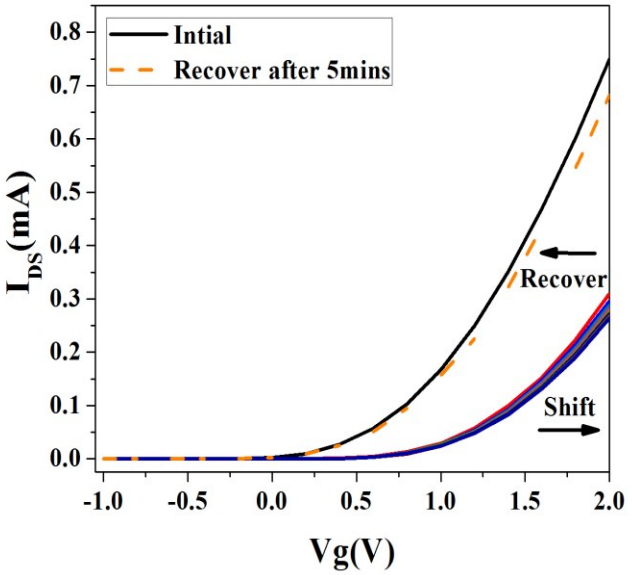
(b)

Figure 2.9 Output characteristics of (a) fresh ZTO FET with SA gate dielectric and (b) ZTO FET with SA gate dielectric after HMDS coating.

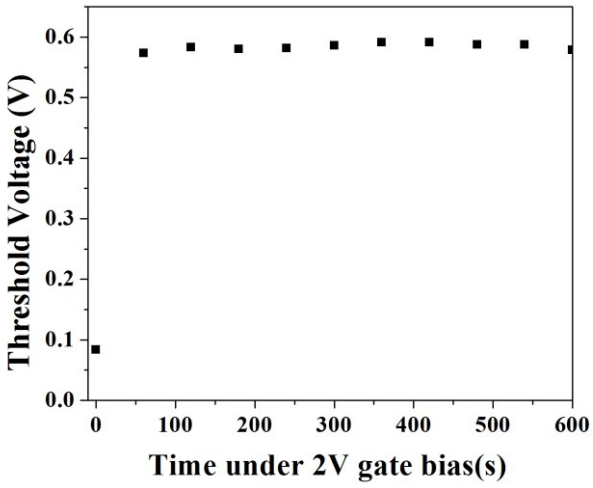
Amorphous semiconductor oxide FETs generally show threshold voltage shift under gate bias. Under gate bias stress, the ZTO becomes more subject to ambient environment elements, such as water, and more charges accumulate to the interface between gate and semiconductor if there are large defect states on the surface of the gate material. A typical transfer curve under 2V gate bias for SA based ZTO FETs is shown in Figure 2.10 (a). We can see from the threshold voltages plotted in Figure 2.10 (c) that threshold voltage shifts from 0.09 V to 0.57 V in the first 60 seconds and stays nearly constant in the next 540 seconds. The absolute value of the threshold voltage shift is not large, only 0.48 V. However, if we consider that the maximum gate voltage is only 2V, the relative shift is quite large, about 25%. The threshold voltage shift is recoverable as shown in Figure 2.10 (b). After 5 min a negative shift of threshold voltage was seen and it is almost overlaps with the original transfer curve. A 10nm Al_2O_3 was coated as a capping layer on SA, but it did not improve gate bias stress stability.



(a)



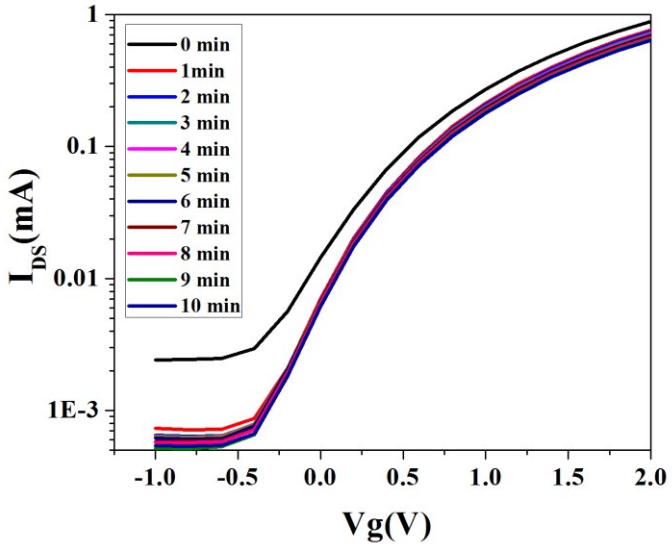
(b)



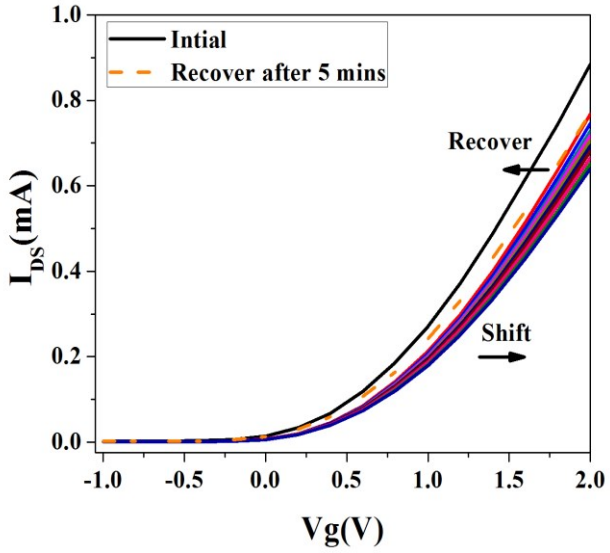
(c)

Figure 2.10 (a) Transfer characteristics of ZTO FET with SA gate dielectric under 2 V gate bias; (b) transfer curve recovery after 5mins; (c) threshold voltage shift under gate bias without Cytop coating.

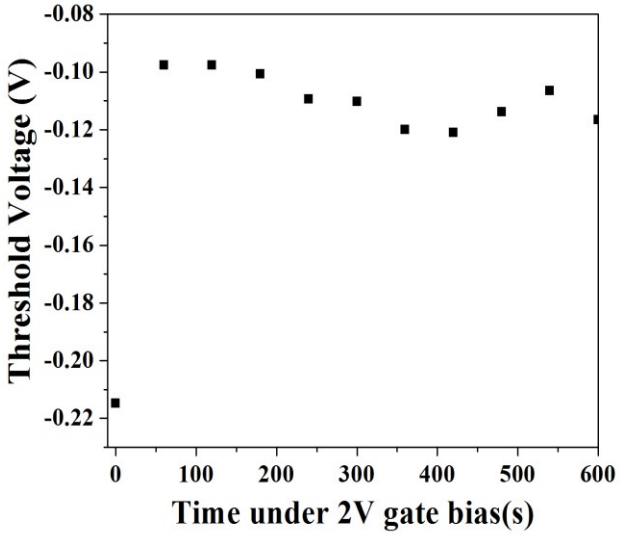
After coating with Cytop, previously used as a barrier coating with inorganic oxide devices,[31] we found that the threshold voltage of SA based ZTO FETs is more stable under gate bias, showing in Figure 2.11 (a). It is clearly shown that transfer curve shift is much less than for the device exposed directly to the ambient environment. As plotted in Figure 2.11 (b), threshold voltage only shifted about 0.1V after 60 seconds and then fluctuates around -0.1 V in the remaining 540s. These results suggested that the absorption of the species in the ambient environment is responsible for the threshold voltage shift.



(a)



(b)



(c)

Figure 2.11 (a) Transfer characteristics of ZTO FET with SA gate dielectric after coating with Cytop under gate bias 2V; (b) transfer curve recovery after 5mins; (c) threshold voltage shift under gate bias with Cytop coating.

2.8 Conclusions

The incorporation of sodium ions significantly impacts the dielectric and morphological properties of sol-gel solution processed SA films. The polarization of sodium ions increase alumina capacitance tremendously. SA also exhibited a smoother surface morphology than plain alumina dielectric. Low gate leakage current in SA film excluded the possibility of ionic leakage current caused by sodium ion diffusion. Thermal stability and interfacial compatibility of the SA and ZTO are excellent. While pristine SA-based FETs lack environmental stability, simple encapsulation with Cytop improves device stability remarkably.

CHAPTER III

Ion dependence of alumina dielectric behavior

3.1 Introduction

The exceptional apparent dielectric constant and gate dielectric performance of sodium alumina (SA) formulations, nominally crystalline but amorphous on supermolecular scales, was discussed in the previous chapter. SA-FETs with both inorganic and organic semiconductors were successfully operated at very low voltage (2 V). The sodium ions were experimentally proved to be necessary for the high capacitance of this gate dielectric. With this discovery, we were motivated to extend the investigation of dielectric properties of other oxides related to aluminas incorporating other alkali metal ions. In this chapter, we will describe the comparative properties of K^+, Li^+, and Na^+ aluminas, which we abbreviate PA, LA, and SA, respectively. We will also discuss the equivalent circuit model of alkali metal ion-incorporated alumina based on impedance measurement and experimental data fitting with theoretical models. Ion-incorporated alumina dielectric behavior is consistent with an ionic conductor in series with an interfacial capacitive layer, in contrast to the bulk capacitive behavior of alumina itself, and somewhat different from our original model. Ion transport is also found to be more facile with K^+ than with Li^+, consistent with their anticipated binding strengths to oxide anion functional groups including water of hydration, and inconsistent with a model requiring ions to burrow through domains of nonintercalated (ion-free) alumina.

3.2 Experimental section

All ion-incorporated aluminas films are were prepared by sol-gel spin-coating method. Aluminum nitrate nonahydrate (Sigma Aldrich) and alkali metal salts, such as potassium metabisulfite (Alfa Aesar), lithium acetate dehydrate (Sigma Aldrich), or sodium bisulfate (Mallinckrodt Chemicals), with 11:1 molar ratio were dissolved into 2-methoxyethanol solvent to make a 0.5 M ion-incorporated alumina precursor solution. The same molar amount of acetylacetone was added into the solution as stabilizer. The mixed solution was then stirred at room temperature for 6 hours. Plain alumina precursor solution with a concentration of 0.5 M was also prepared with a similar procedure. The only difference in preparing plain alumina precursor and ion-incorporated alumina precursors is that there is no alkali metal ion salt added in the plain alumina precursor. As-prepared precursor solution was kept for 24 hours to promote hydrolysis and filtered through a 0.45 μm PTFE filter.

ZTO solution precursor was prepared by dissolving zinc acetate anhydrous (Alfa Aesar, 0.3 M) and anhydrous tin(II) chloride (Alfa Aesar, 0.3M) into 2-methoxyethanol solution. Acetylacetone (0.6 M) was added into the solution as stabilizer. The mixed solution was then stirred at room temperature for 12 hours. As-prepared precursor solution was kept for 24 hours to promote hydrolysis and filtered through a 0.45 μm PTFE filter.

For field-effect transistors, Alumina solution was spin-coated onto ITO glass substrate (Delta technologies Ltd., CB-90IN-1105, Display Grade Corning 1737 aluminosilicate glass with about 30 nm ITO coating, RMS roughness of the ITO according to Delta is about

1 nm, measured by Atomic Force Microscope) at 5000 rpm for 30 seconds two times and then annealed at 300°C for 30 minutes. In this device structure, ITO works as a gate electrode. The alumina film thickness were measured by profilometer (Dektak IIA) and verified by Filmetrics thin film analyzer (F20). For all ion-incorporated alumina films (LA, SA, and PA), the measured thickness are about 80 nm.

ZTO precursor solution was then spin-coated onto dielectric film at 5000 rpm for 30 seconds. After curing at 75 °C for 15 min, the same process was repeated again and the as-deposited film was annealed at 500 °C for 1 hour. Afterwards, aluminum (100 nm) was deposited by thermal evaporation as source and drain electrodes. Slim-bar TEM grids (SPI Supplies, 200 mesh) were used as a shadow mask and the typical channel width (W) is about 100 μm and channel length (L) is 10 μm.

For metal-insulator-metal capacitors, ITO was used as the bottom electrode and thermally evaporated aluminum was used as the top electrode. Dielectric layer was prepared by spin-coating alumina solution onto ITO glass substrate (Delta technologies Ltd., CB-90IN-1105, Display Grade Corning 1737 aluminosilicate glass with about 30 nm ITO coating) at 5000 rpm for 30 seconds. In dielectric behavior analysis alumina precursors were spin-coated one time or three times. All dielectrics films in MIM capacitors were finally annealed at 500 °C for 1 hour, and so this procedure is comparable to FETs annealed at 500 °C for 1 hour. For one time coated dielectrics, samples were annealed at 500 °C for 1 hour right after spin-coating. For three times coated dielectrics, samples were annealed at 300 °C for 30 min after first and second spin-coating, and final annealed at 500 °C for 1 hour after third spin-coating.

Electronic properties of FETs were analyzed using an Agilent 4155C semiconductor parameter analyzer. The equivalent circuit model for ion-incorporated aluminas in the frequency region from 100 Hz to 100 kHz was determined by analyzing electrochemical impedance spectra of ion-incorporated alumina MIM capacitors. The impedance measurement was performed using a Solartron 1260 impedance analyzer and Solartron 1287 electrochemical interface controlled by ZPlot and ZView software. A semicircle on the complex impedance plot was observed in both PA and LA capacitors measured at 275 °C, this indicates an equivalent circuit with a resistor and a capacitor in parallel.

Based on this, the parallel circuit model was chosen for analysis of MIM capacitors using an Agilent 4284ALCR meter. Both temperature and humidity were controlled during the measurement. AC conductivity was calculated according to the following equations:

$$Z' = \frac{R_p}{1+\omega^2 C_p{}^2 R_p{}^2}, \quad Z'' = \frac{-j\omega C_p R_p{}^2}{1+\omega^2 C_p{}^2 R_p{}^2}, \quad \sigma_{ac} = \frac{Z'd}{A[(Z')^2+(Z'')^2]}$$

Z' is the real part of the impedance, Z'' is the imaginary part of impedance, d is the thickness of dielectric layer, and A is the area of the top electrode of the MIM capacitor.

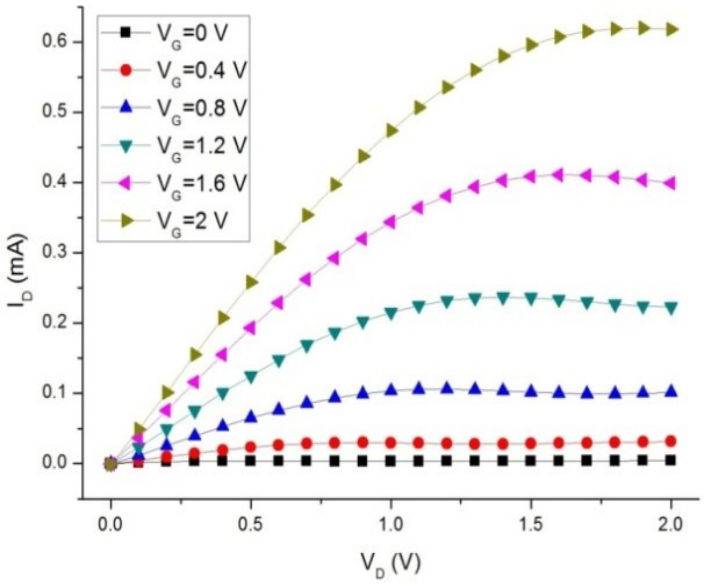
The concentration of alkali metal ions in ion-incorporated alumina films was analyzed with a secondary ion mass spectrometer (Cameca IMS 6f). O^{2+} at 5.5 keV impact energy was used as the primary ion for SIMS analysis. To prevent voltage-induced alkali metal ion movement and improve secondary ion extraction, a gold layer was coated on top of ion-incorporated aluminas for charge neutralization. Li^+ ions were implanted in an aluminum oxide film to make a standard sample for Li^+ ion calibration. SIMS depth profile on the implanted sample showed that the gold layer was sufficient for charge neutralization.

K^+ and Na^+ concentration were estimated based on the assumption that Li, K, and Na have similar sensitivity factors.

3.3 Performance of FETs with PA and LA gate dielectrics

Output and transfer characteristics of PA- and LA-based FETs with zinc tin oxide (ZTO) semiconductor were measured at 0-2 V as shown in Figure 3.1. In Figure 3.1 (a) and Figure 1 (c), drain current saturated at a very low voltage showing effective pinchoff behavior. At 2 V gate voltage, saturated drain current varied from 0.65 mA to 1.2 mA with different W/L ratios. This current is close to what we reported in ZTO FETs with SA gate dielectric.[1,2] Leakage current was negligible compared with saturation drain current at 2 V gate voltage.

Figure 3.1 (b) and (d) show representative transfer characteristics of FETs with PA and LA dielectrics respectively. As gate voltage increased, the increased drain current showed a good fit to the square relation in the saturation drain current equation. The turnon voltage is on the depletion side of zero. The highest saturation-region field-effect mobility obtained was about 20 $cm^2V^{-1}s^{-1}$, which compares well with the saturation-region field-effect mobility of solution-processed ZTO reported by other groups.[3-8] A low subthreshold swing (about 200 mV/decade) was achieved in both FETs, which indicates low interface trap density in the ZTO films.[9-10] This result is based on the measurement of 60 transistors on 12 bilayer films for LA and PA gate dielectrics respectively. Detailed information of FET electrical performance is summarized in Table 3.1. Plots of device hysteresis are shown in Figure 3.2. The hysteresis in the accumulation regime is minimal. Also, off current was lowered to just 1 nA by using thinner ZTO films shown in Figure 3.2 (c), (d). The reduced off current could be attributed to a reduced defects and interfacial charges.


V_G=0 V
V_G=0.4 V
V_G=0.8 V
V_G=1.2 V
V_G=1.6 V
V_G=2 V
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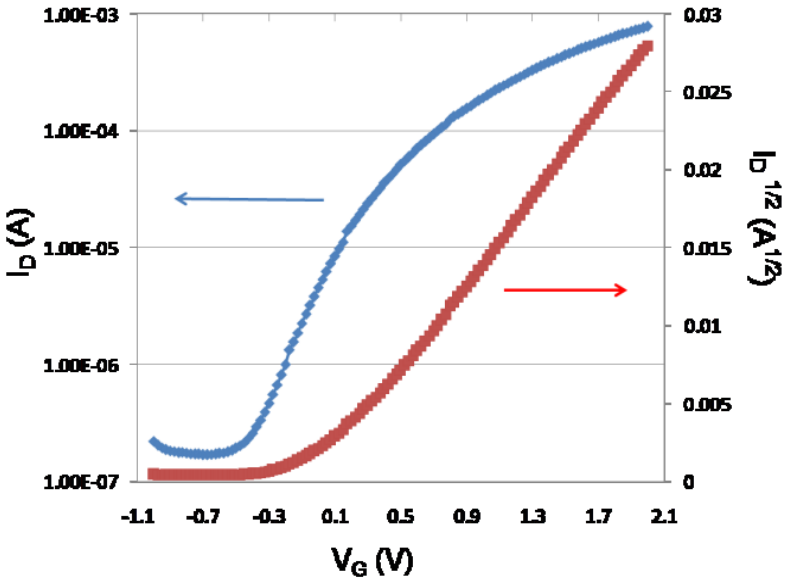
V_D (V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.0
0.5
1.0
1.5
2.0

(a)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1.00E-04
1.00E-05
1.00E-06
1.00E-07
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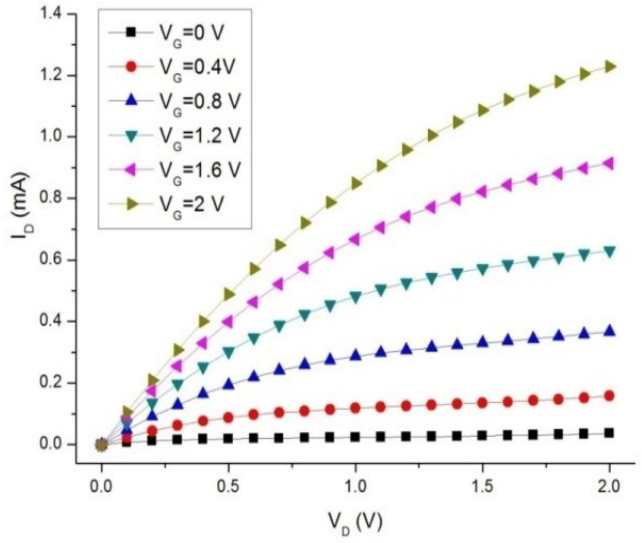
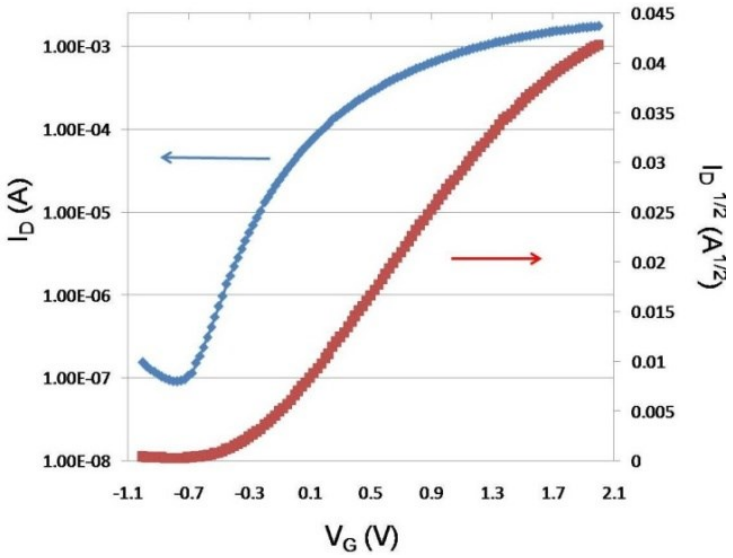
0.025
0.02
0.015
0.01
0.005
0
I_D^1/2 (A^1/2)
-1.1
-0.7
-0.3
0.1
0.5
0.9
1.3
1.7
2.1
V_G (V)

(b)

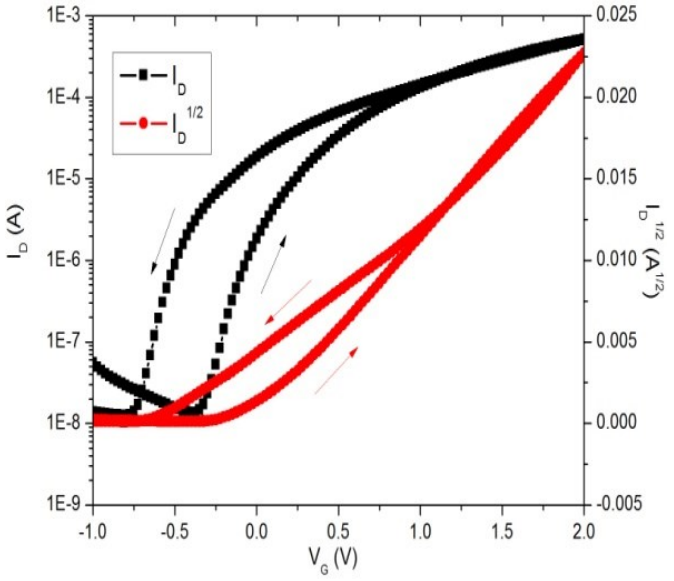


(c)



(d)

Figure 3.1 Output and transfer characteristics of ion-incorporated alumina-based FETs with ZTO as semiconductor. (a) Output characteristics of PA based FET; (b) transfer characteristics (log and square root) of PA based FET; (c) output characteristics of LA based FET; (d) transfer characteristics of LA based FET.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1E-6
1E-7
1E-8
1E-9
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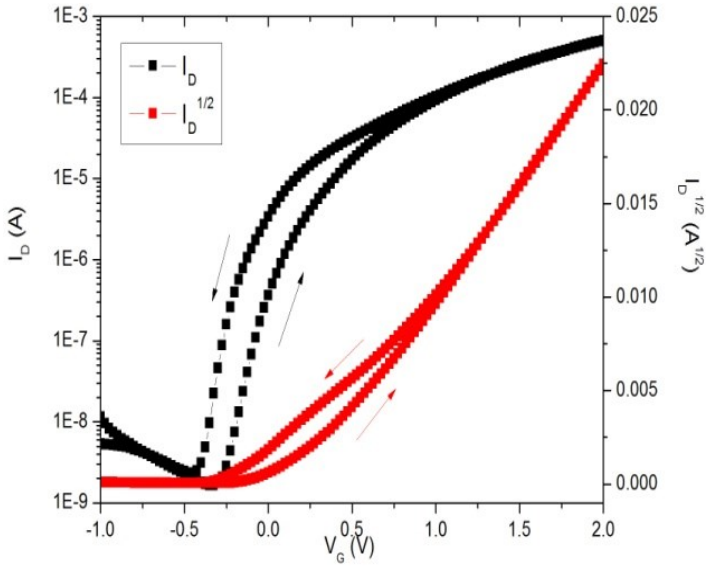
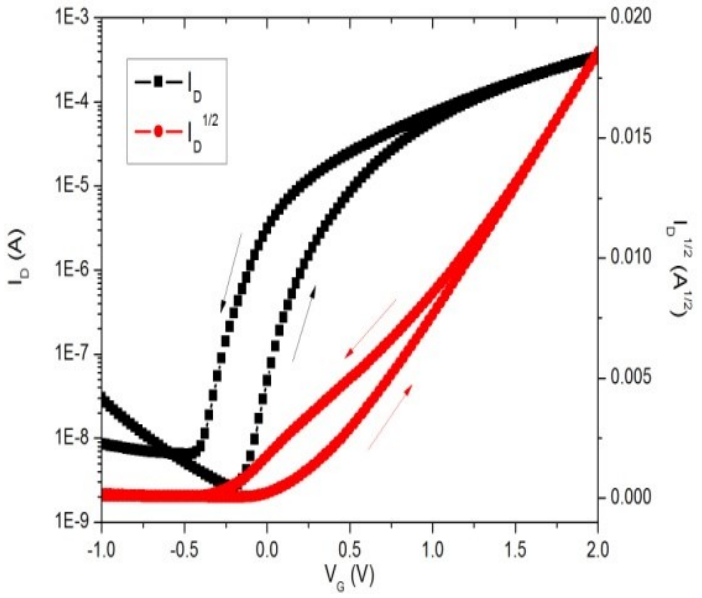
0.020
0.015
0.010
0.005
0.000
-0.005
I_D^1/2 (A^1/2)
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0
V_G (V)
I_D
I_D^1/2

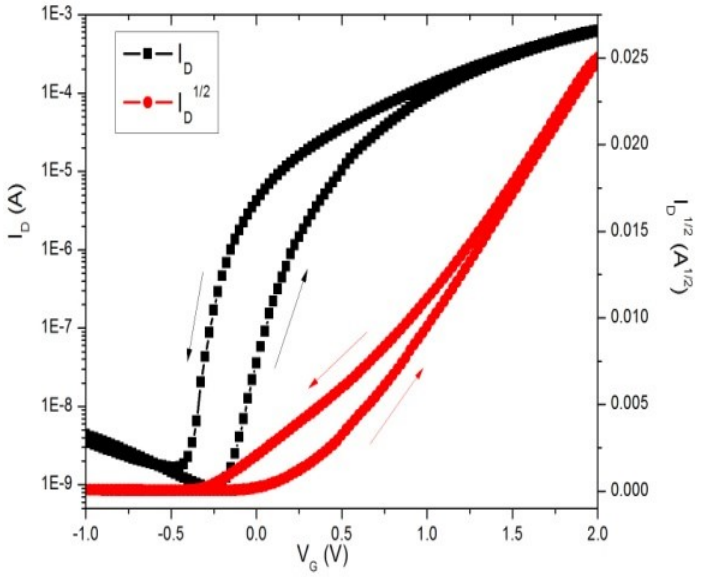
(a)


1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
I_D (A)
0.025
0.020
0.015
0.010
0.005
0.000
I_D^1/2 (A^1/2)
-1.0
-0.5
0.0
0.5
1.0
1.5
2.0
V_G (V)
I_D
I_D^1/2

(b)



(c)



(d)

Figure 3.2 Hysteresis in transfer curves of (a) PA and (b) LA transistors with ZTO as semiconductor (80 nm). FET transfer curves of (c) PA and (d) LA transistors showing lower off current with thinner ZTO layers (40 nm).

Table 3.1 Electrical performance of PA and LA based FETs shown.

	W/L	V_{th} (V)	μ_{sat} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	SS (mV/decade)	I_{on}/I_{off}
PA	**11**	**-0.007**	**16.1**	**294**	**5×10^3**
LA	**18**	**-0.3**	**19.6**	**201**	**2×10^4**

3.4 Leakage current of SA, PA, LA, and Al_2O_3 MIM capacitors

Leakage current is a critical parameter to evaluate ion-incorporated alumina dielectric behavior. In low-voltage portable devices, leakage current should be minimized not only for reducing energy consumption but also for improving switching efficiency of transistors. We measured leakage current by applying voltage to an aluminum contact to the bottom ITO substrate, while grounding the Al top electrode.

As shown in Figure 3.3, the leakage currents of ion-incorporated alumina capacitors were similar to each other and about an order of magnitude higher than for the Al_2O_3 capacitor. The dielectric layer thickness is about 80 nm for all capacitors. This behavior could be attributed to the diffusion of polarized alkali metal ions in the alumina matrix, as discussed further below. This does not prevent effective transistor switching. The quality of our sol-gel spin-coated Al_2O_3 dielectric film is comparable to vacuum deposited Al_2O_3 dielectric, as the leakage current of Al_2O_3 dielectric shown in Figure 2 is similar to that of Al_2O_3 dielectric fabricated by a vacuum deposition method.[11]

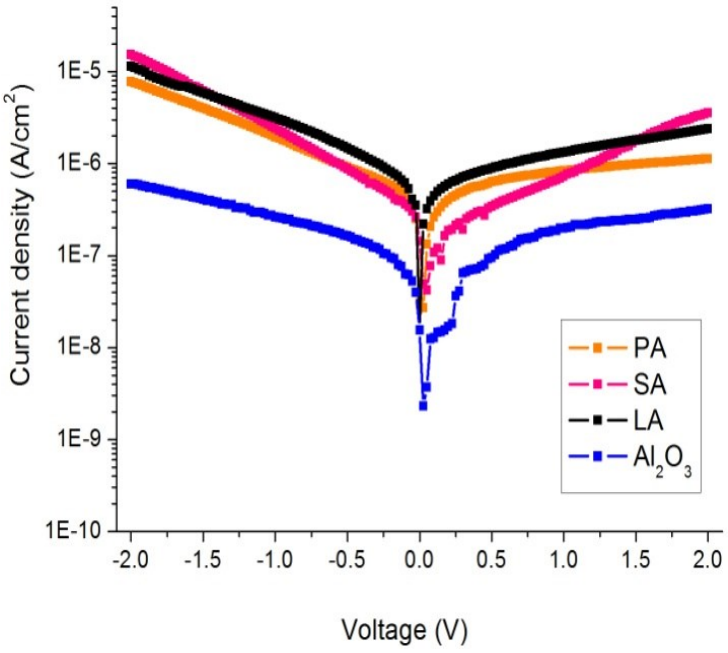


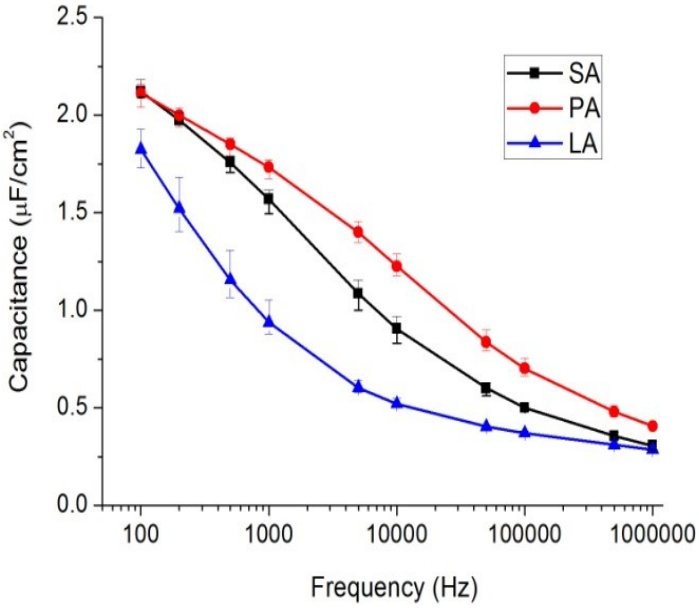
Figure 3.3 Leakage current of ion-incorporated alumina MIM capacitors and Al_2O_3 MIM capacitor.

3.5 Frequency dependence of capacitance and AC conductivity of SA, PA, and LA MIM capacitors

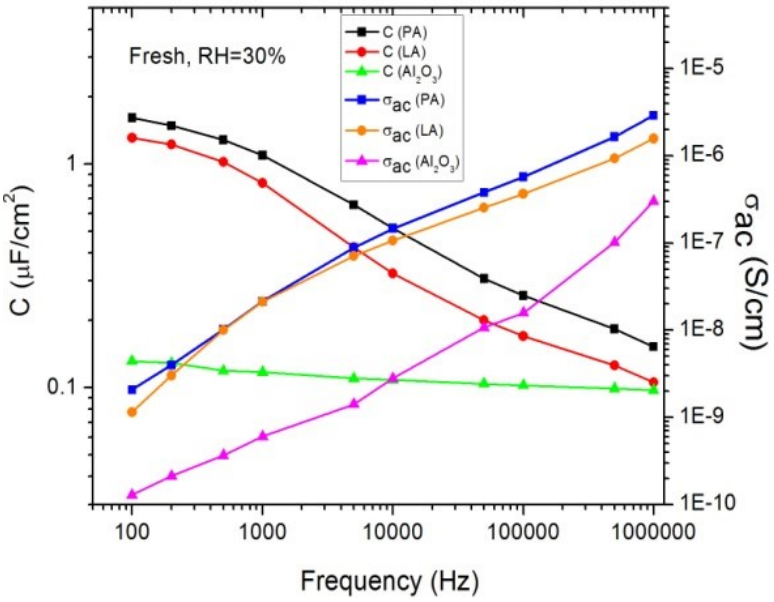
To investigate the effect of the nature of the alkali metal ion on alumina dielectric properties, metal-insulator-metal (MIM) capacitors with different alkali metal ions were analyzed with an Agilent 4284A LCR meter at controlled temperature and humidity.

Figure 3.4 shows the capacitance of alumina MIM capacitors with Li^+, Na^+, or K^+ ions in a frequency range from 100 Hz to 1 MHz measured at room temperature and at 30% relative humidity. Additional plots, comparing both capacitance and AC conductivity of alumina, LA, and PA, are included as well. Points reflect averages of five devices for each type of alumina. Values dropped somewhat on aging, with LA capacitance dropping

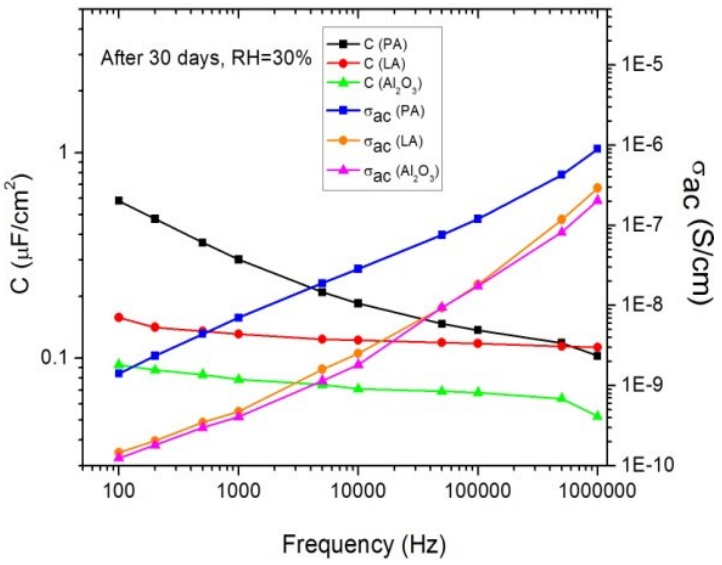
substantially at low frequency and conductivity dropping at all frequencies. LA and PA conductivities were an order of magnitude higher than alumina itself in fresh samples, consistent with the leakage current data of Figure 3.3. PA and SA capacitances differed by 0-30% depending on frequency. LA had two times less capacitance than PA at intermediate frequencies, but only 20-30% less capacitance at the lowest and highest frequencies. As will be seen later, the film thickness was not a major determining factor in the capacitance.



(a)



(b)



(c)

Figure 3.4 Capacitance of ion-incorporated alumina MIM capacitors at different frequencies (a), and comparison of capacitance and AC conductivity of fresh (b) and aged (c) samples of alumina, LA, and PA. The dielectric thickness of all samples is about 80 nm.

The high capacitance ($2\mu F/cm^2$) achieved at low frequency compared to plain alumina might be explained by formation of an electric double layer by the polarization of alkali metal ions at the alumina/Al interface.[12-16] Also, the capacitance at all but the extreme frequencies is highest for PA, where K^+ is the least covalently bound included ion of the three. The capacitance of LA moves toward that of alumina on aging, while that of PA does not, also a presumed consequence of the differences in ion-oxygen binding, possibly coupled to a reorganization of channel morphology. In the frequency ranges studied so far, there are hints of the expected leveling of capacitance at high frequency as bulk capacitance dominates, and a second leveling at low frequency in the ionic materials as an interfacial double layer becomes established as the dominant capacitance. This electrical model was not contemplated in our original hypothesis, but may effectively explain many of our observations.

The capacitance and frequency relationship that we observe is typical in electric double layer capacitors.[12, 15-20] These double layers typically exist at the interface between electrode and electrolyte. At high frequency, ion migration to form the double layer is impeded, and thus the measured capacitance reflects the bulk capacitance of the sample. For plain alumina dielectric, the calculated capacitance of 80 nm Al_2O_3 (ε=9.2) matrix material is about 0.1 $\mu F/cm^2$, and this value is close to the high frequency capacitance shown in Figure 3.4 (a).

The ion dependence of the double layer capacitance in our ion-incorporated alumina capacitors would be determined by factors such as ionic polarizability interfacial ion density, ion-ion interaction, ion-oxygen binding, and ion-electrode interaction. For example, the greater polarizability of K^+ relative to Li^+ may have resulted in greater double

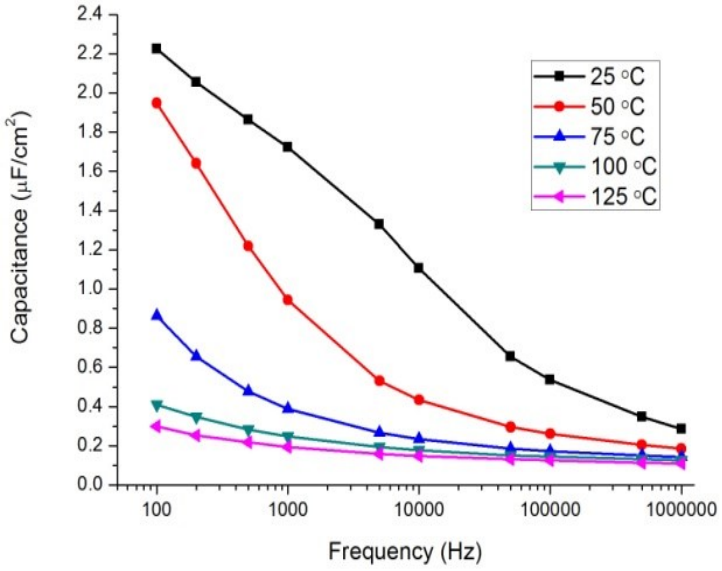
layer capacitance for K^+. Alternatively, the easier migration of hydrated K^+ through channels relative to Li^+ might have led to higher K^+ capacitance at a given frequency because of the more complete formation of the K^+ double layer at that frequency.

No frequency-independent conductivity region was observed in Figure 3.4. All alumina dielectrics analyzed show the Jonscher type power law frequency dependence of AC conductivity:[21-23] $\sigma(\omega) \propto \omega^n$, $n \leq 1$. This is a universal AC conductivity behavior in ion conducting disordered solid materials, and is further evidence for the ionic migration causing the observed leakage currents. Compared to plain alumina, ion-incorporated aluminas showed a higher AC conductivity; this could be attributed to the alkali metal ion contribution in ion-incorporated aluminas. In ion-incorporated aluminas, lower AC conductivity was observed in LA. This may be because stronger Li-oxygen binding could impede Li ion conduction in the alumina channels more significantly. An alternative explanation is that the known larger hydration radius of Li ion decreases ion mobility in confined geometries.[24, 25]

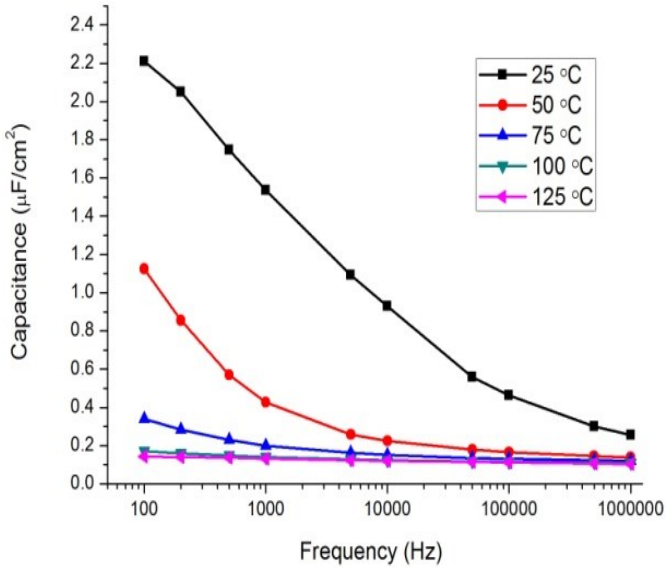
3.6 Thickness and temperature dependence of capacitance and AC conductivity of SA, PA, and LA MIM capacitors

To analyze thermally induced alkali metal diffusion in Al_2O_3 matrix material, dielectric properties of ion-incorporated alumina MIM capacitors were measured in a temperature range from 25 °C to 125 °C at 30% relative humidity (Figure 3.5) In Figure 3.5 (a), (b), and (c), the measured capacitance remains almost constant throughout the frequency range at 125 °C, and this capacitance is very close to the capacitance of the 80 nm thick Al_2O_3 (ε=9.2) matrix material. The reason may be the decreased effectiveness of water in

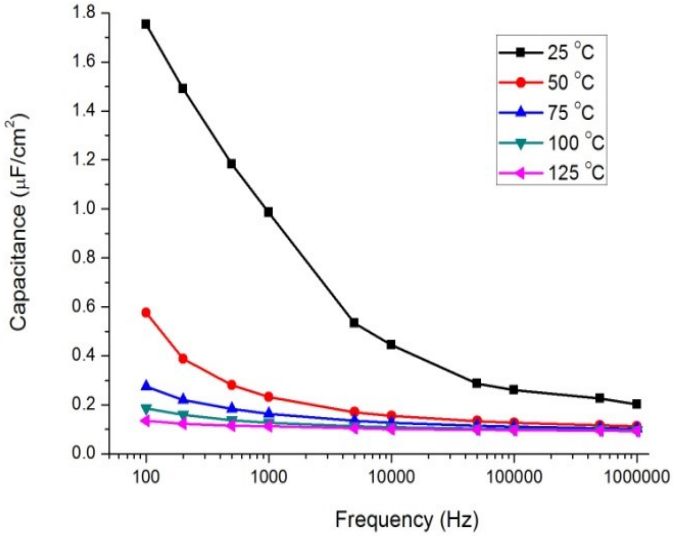
promoting the diffusion and/or polarization of ions (even at constant humidity) at the higher temperature, an effect that also influences capacitance. Figure 3.5 also shows increased temperature dependence, and therefore activation energy, of capacitance with decrease in the ionic radius of the included ions, again consistent with stronger binding of the smaller ions to the oxide groups in the channels or to a larger number (or temperature dependence of the number) of water molecules in a hydration shell. Figure 3.5 (d) shows the capacitance of an Al_2O_3 MIM capacitor. At room temperature, the low frequency capacitance of Al_2O_3 is more than one order of magnitude lower than that of ion-incorporated alumina capacitors. Compared with ion-incorporated alumina capacitors, Al_2O_3 capacitance was much less affected by temperature change and it was almost independent of frequency.



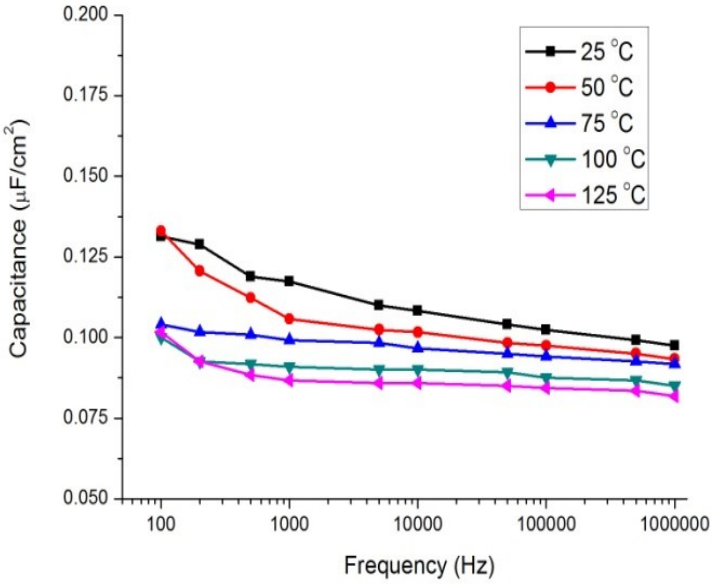
(a)


Capacitance (μF/cm²)
Frequency (Hz)
25 °C
50 °C
75 °C
100 °C
125 °C

(b)


Capacitance (μF/cm²)
Frequency (Hz)
25 °C
50 °C
75 °C
100 °C
125 °C

(c)

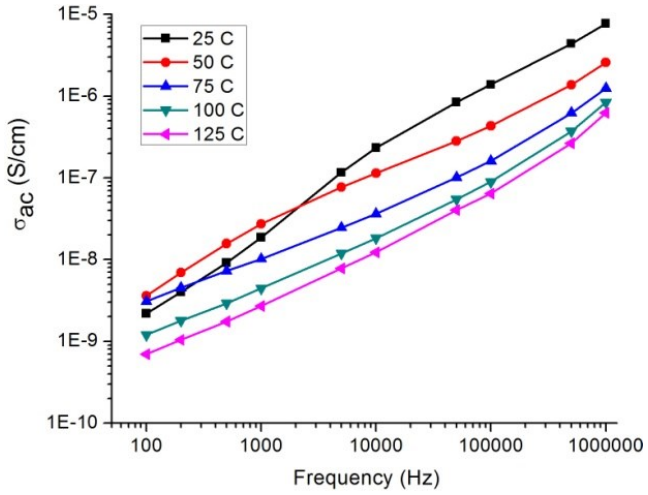


(d)

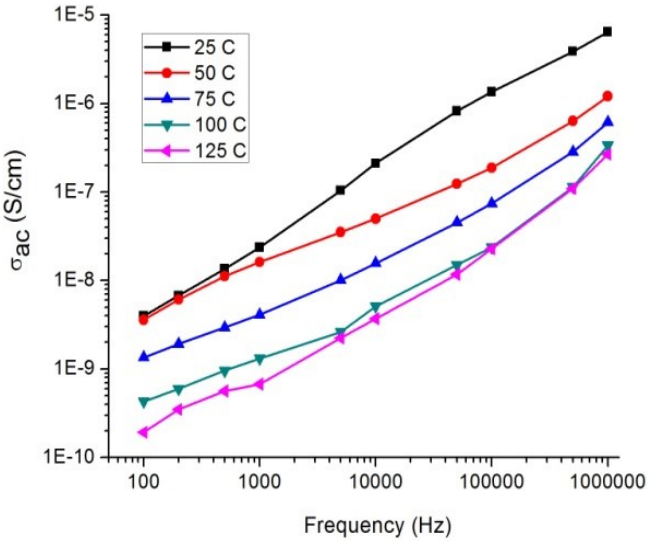
Figure 3.5 Temperature dependence of capacitance of ion-incorporated alumina and plain alumina MIM capacitors. (a) PA capacitor; (b) SA capacitor; (c) LA capacitor; (d) Al_2O_3 capacitor. The dielectric thickness is about 80 nm for all samples.

Figure 3.6 shows the AC conductivity of both ion-incorporated aluminas and plain alumina in the temperature range from 25 °C to 125 °C. An anomalous decrease in AC conductivity with the increase of temperature was observed in aluminas. Generally, high temperature promotes ion conduction in disordered solids and the DC conductivity is Arrhenius temperature dependent.[22, 23] However, our alumina samples are humidity-sensitive. The decrease of moisture level as temperature increases would reduce ion solvation and this could be the origin of low AC conductivity measured at high temperature. Due to the lack of alkali metal ion in plain alumina, no obvious temperature dependence on AC conductivity was observed. A significant increase in conductivity at high relative

humidity level was also observed by adding alkali metal ions (Li^+, K^+) into TiO_2 films.[26, 27] Proton hopping transport induced by water absorption was not sufficient to explain the enhanced conductivity. The explanation proposed was that the water adsorption decreases the activation energy for alkali ion diffusion in the TiO_2 film.



(a)



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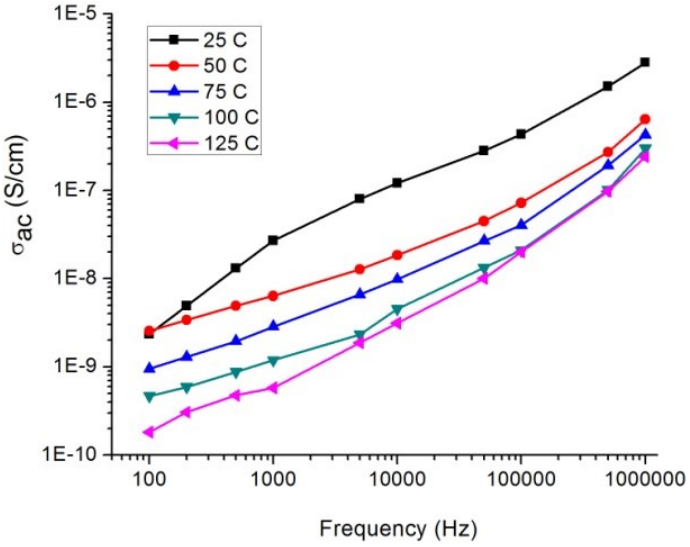

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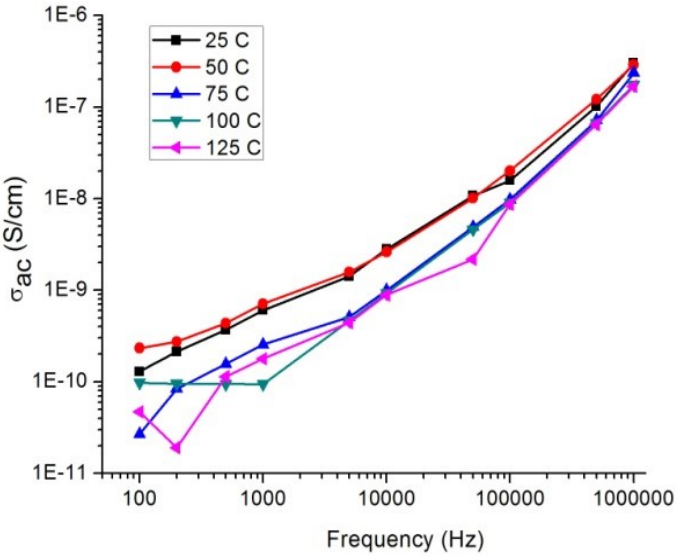
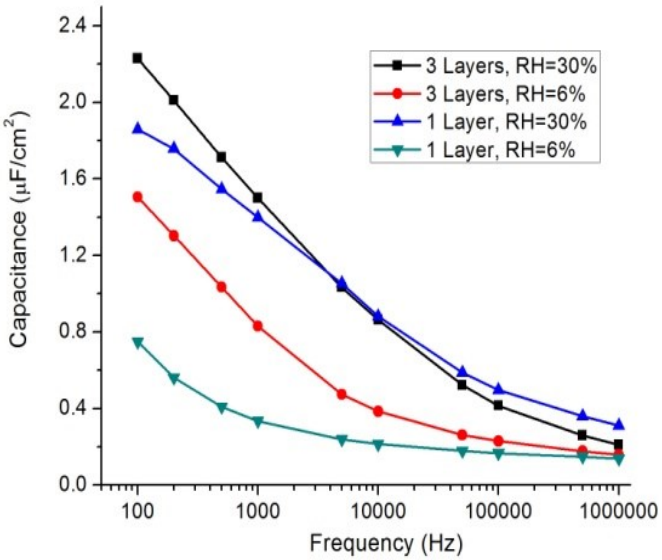


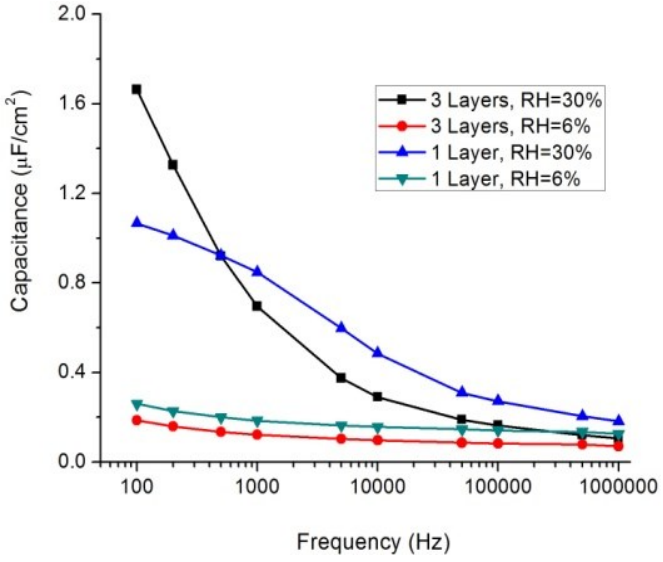
(d)

Figure 3.6 Temperature dependence of AC conductivity of ion-incorporated alumina and plain alumina MIM capacitors. (a) PA capacitor; (b) SA capacitor; (c) LA capacitor; (d) Al_2O_3 capacitor. The dielectric thickness is about 80 nm for all samples.

Figure 3.7 shows comparisons of capacitance of ion-incorporated alumina capacitors with alumina capacitors at different layer thicknesses and under different relative humidities. Ion-incorporated alumina dielectric films with a thickness range from about 40 nm to 120 nm (ion-incorporated alumina spin-coated 1 time or 3 times) were fabricated and sandwiched between two aluminum electrodes. A small variation in capacitance of devices with different thickness was observed for PA but the capacitance did not show a linear dependence of ion-incorporated alumina thickness as described in the capacitance equation for a classic parallel flat plate capacitor. On the other hand, the alumina samples did show the expected thickness dependence. This indicates that the electrical models for the two cases are different, with the alumina acting as a bulk capacitor and the ion-incorporated aluminas acting as double layer capacitors in the low frequency limit and as bulk capacitors only in a very high frequency limit, possibly indicated by the crossing of the PA 1-layer and 3-layer curves.



(a)



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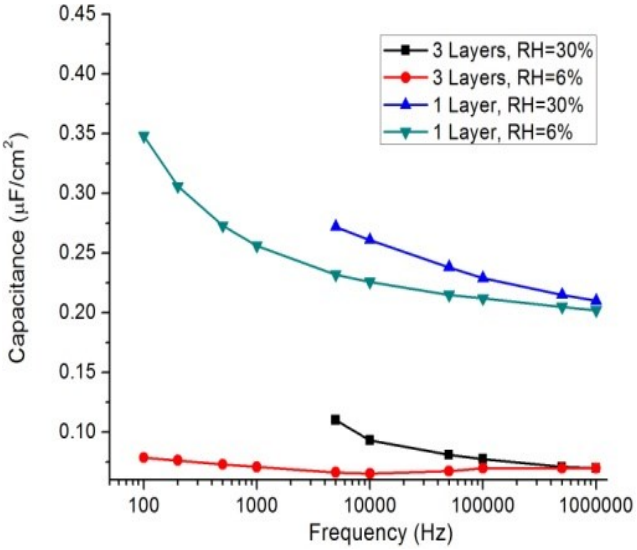
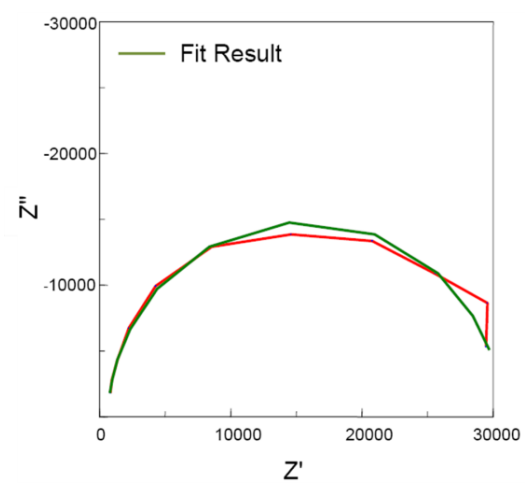
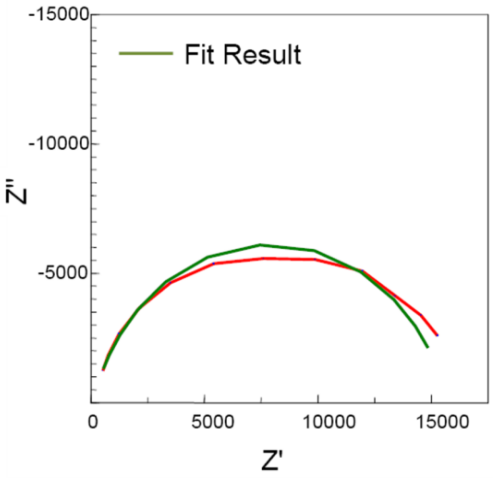


(c)

Figure 3.7 Thickness dependence of capacitance of ion-incorporated alumina MIM capacitors at RH=30% and RH=6%. (a) PA capacitor; (b) LA capacitor; (c) Al_2O_3 capacitor.



(a)



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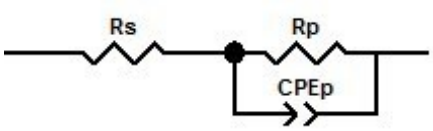


(c)

Figure 3.8 Original (red curve) and simulated (green curve) Nyquistplots for LA (a) and PA (b) MIM capacitors and equivalent circuit (c) used for impedance simulation.

Complex impedance measurements were made within the frequency range 100 Hz-100 kHz, where semicircular plots of Z'' vs Z' consistent with parallel capacitor-resistors in series with a small DC resistance were obtained (Figure 3.8). A strong humidity dependence of capacitance and a weak dielectric thickness dependence of capacitance had also been observed previously in LiF MIM capacitors.[28] That behavior was explained by the formation of a double layer structure with water-induced diffusion of lithium ions toward the cathode/LiF and diffusion of fluoride ions toward the anode/LiF interface.

3.7 Capacitance behavior of ion exchanged ion-incorporated aluminas

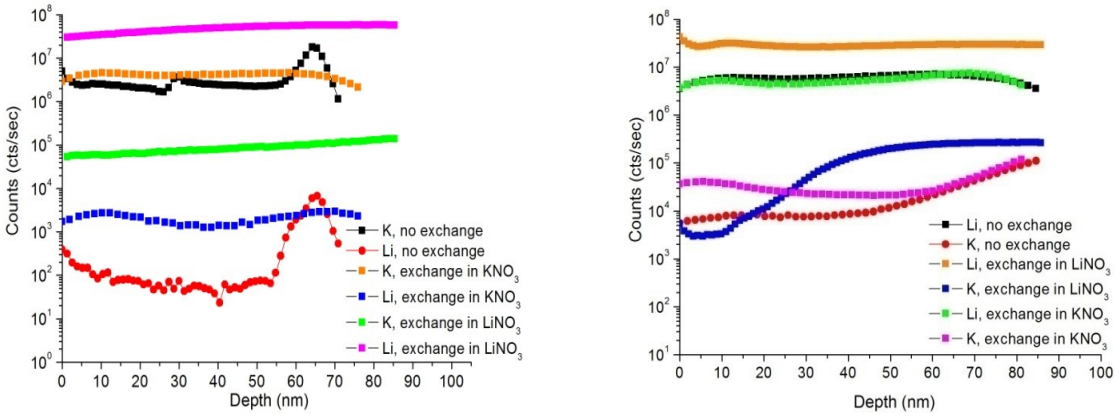
Ion exchange experiments were conducted to investigate alkali metal ion diffusion behavior in ion-incorporated aluminas. As a general procedure, as-deposited ion-incorporated alumina films were immersed in 0.1 M alkali metal nitrate solution (KNO_3 or $LiNO_3$) for 20 hours. After that, films were rinsed with deionized water and aluminum electrodes were then deposited by thermal evaporation.

A PA film was immersed into 0.1 M lithium nitrate solution for 20 hours. In addition, a control sample was prepared by immersing PA film in 0.1 M potassium nitrate solution for 20 hours. The same procedure was repeated to study ion exchange behavior of LA films. Alkali metal ion depth profiles of both PA and LA films with different ion exchange conditions were analyzed by secondary ion mass spectrometry (SIMS). Ion concentration depth profiles of PA and LA films without ion exchange were also analyzed for comparison.

Figure 3.9 (a) shows the alkali metal ion depth profiles of the different PA films. Generally, alkali metal ion concentration is found to be relatively constant throughout the 80 nm thick ion-incorporated alumina films. A small ion concentration variation was observed for the unexchanged sample near the interface with the substrate and this may be attributed to ion movement induced by the voltage applied during measurement. On exchanging with Li, a significant amount of Li^+ ions diffused from the LiNO3 solution into PA film, while a smaller amount of K^+ ions diffused out from the film. Li^+ has a smaller ionic weight and size than K^+ and thus Li^+ would have a higher diffusion rate and a smaller probability to be repelled by other cations already in the PA film, assuming their waters of hydration were equally exchangeable. When ions in the PA film were “exchanged” with KNO_3 solution, no remarkable change in potassium concentration was observed, indicating

that any sites available for K^+ binding were occupied during the original sample preparation and stably bound; otherwise, an adjustment of K^+ concentration in the film would have been observed.

SIMS depth profiles of LA samples are shown in Figure 3.9 (b). As expected, the Li concentration of the unexchanged LA film was of the same order as the K concentration in the unexchanged PA sample shown in Figure 3.9 (a). Diffusion of Li^+ ions from $LiNO_3$ solution into to LA film was observed, in contrast to the case with K^+. However, the ion concentration gradient between LA film and KNO_3 solution was unable to promote exchange or incorporation of Li^+ or K^+ ions, respectively. This is evidence for structural and binding differences between the two ion-incorporated aluminas. The structure of amorphous oxides is described to be a random network composed of polyhedra. In ion-incorporated aluminas, the size and connectivity of polyhedra in the Al_2O_3 matrix would be influenced by the type of alkali metal ion incorporated. In turn, the Al_2O_3 matrix structure affects ion motion inside one polyhedron and between polyhedra.



(a) (b)

Figure 3.9 SIMS depth profile of PA (a) and LA (b) before and after ion exchange with Li^+ or K^+ in nitrate solution for 20 hours. Legends indicate ions examined by SIMS.

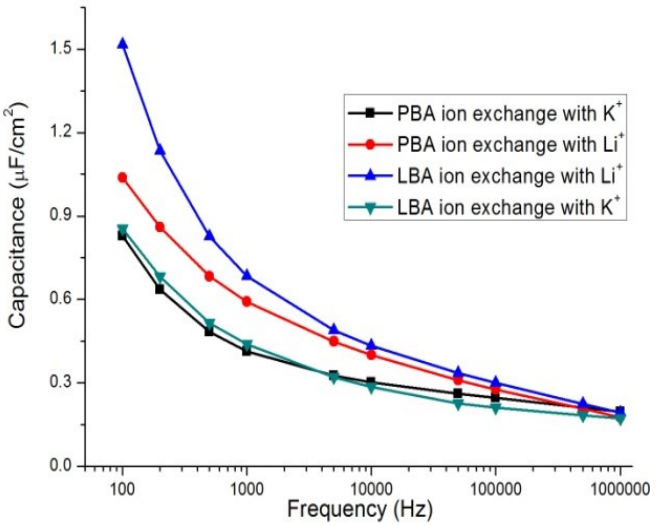


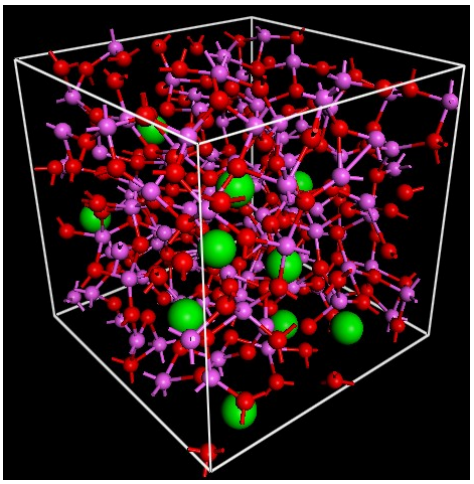
Figure 3.10 Capacitance of PA and LA MIM capacitors after ion exchange with Li^+ or K^+ in nitrate solution for 20 hours. The dielectric thickness is about 80 nm for all samples.

Figure 3.10 shows the capacitance of ion-incorporated alumina capacitors after ion exchange in either $LiNO_3$ or KNO_3 solution after 20 hours. In both cases, ion-incorporated aluminas ion-exchanged in $LiNO_3$ solution showed a higher capacitance than those exchanged in KNO_3 solution. This behavior could be interpreted by the remarkable increase of Li^+ concentration after ion exchange in $LiNO_3$ solution as observed in SIMS analysis. This could also be related to the change of alkali metal ion distribution in the double layer caused by deforming the amorphous Al_2O_3 matrix structure during soaking in nitrate solution, or the presence of enough water after the exchange so that hydration shell water no longer limits ion migration.

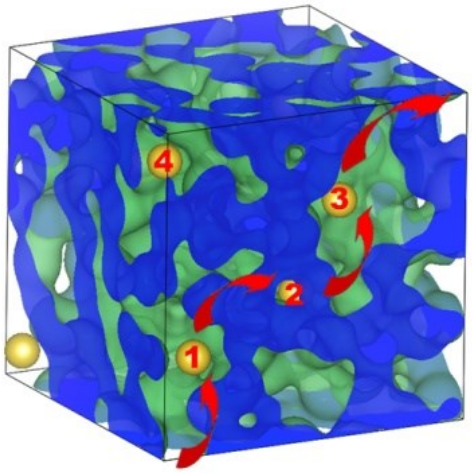
3.8 Structural modeling

A melt-quenching method was used to computationally construct plausible structures for our ion-incorporated alumina solids. This was accomplished using the VASP [29-31] to

perform ab initio molecular dynamics calculations on samples consisting of 110 aluminum atoms, 170 oxygen atoms and 10 ions. The system was intialized in a liquid state and the temperature was lowered at a rate of 10 K/ps to produce an amorphous structure. The resulting radial distribution function was compared to experimental data and found to be nearly identical to that of amorphous alumina. We investigated the effect of the presence of various ions (Na^+, Li^+ or K^+) during the quench on the barriers to ion migration within the amorphous alumina structure. The structures obtained are shown in Figure 3.11.



(a)



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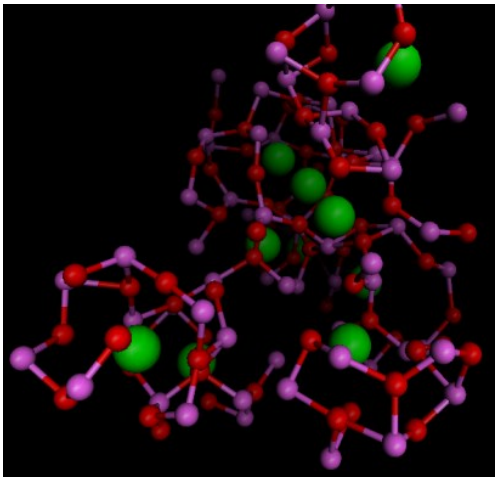

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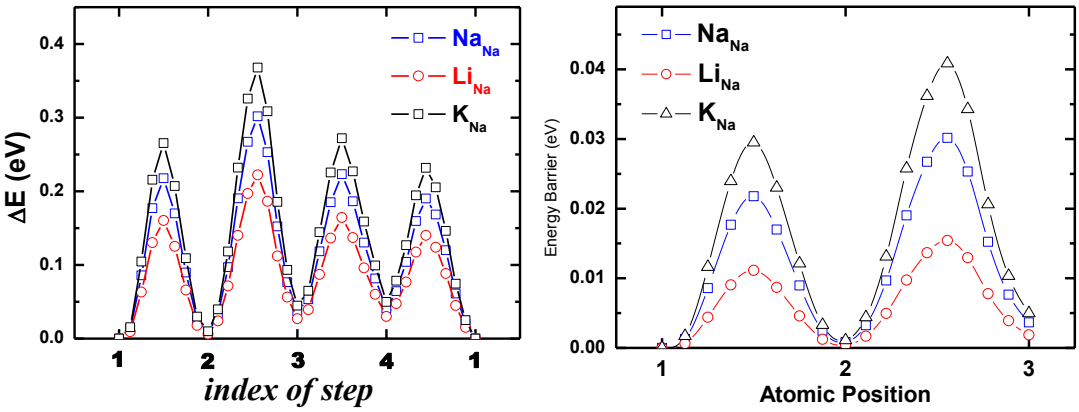


(d) (e)

Figure 3.11 (a) Pore/channel structures obtained from simulation of SA. (b) The possible transport path for an ion through a series of pores with pores labeled 1-4. (c) Multiple ions occupying a single pore illustrating the presence of multiple sites with a pore. (d) Plots of activation energies for ion transfer between pores (from positions 1-4 in the contour diagram) and (e) among three positions in one pore (indicated by the yellow arrow in the pore detail structure) in a structure originally quenched in the presence of Na^+ ions.

Regardless of whether the included ions were Li^+, Na^+, or K^+, the ions were found to occupy pores in the amorphous alumina structure. The activation barriers for transport were found to depend much more significantly on the nature of the ion than on the differences in the alumina structure that arose due to the ion present during the quench. Activation energy differences between Li^+ and K^+ for interpore transfer were on the order of 0.1 eV (4kT where k is the Boltzmann constant, T=298 K), and 0.025 eV (kT) for intrapore position exchange. Values for Na^+ were between those of Li^+ and K^+, and closer to K^+. Activation energy differences of 0.1 eV would indicate transport rates differing at 298K by a factor of 50, far greater than and in the opposite sequence (Li^+ relative to Na^+ relative to

K^+ conductivity) to what we actually observe. The magnitudes of our observed differences are much closer to factors of 2, consistent with activation energy differences on the order of kT, though again in the opposite sequence. This leads us to infer that in the actual structures, which are solution processed rather than melt-quenched, pores form a connected structure although they do not coalesce into the lamellar crystalline structure typical of sodium alumina. As a result the lower, intrapore activation barriers are closer to the actual barriers for transport observed in our structures. A reasonable explanation of the inverse dependence of our barrier heights on the ion species is that the simulation neglected the presence of water, and the smallest ion moved with the least barrier. Because our experiments were largely performed under conditions of finite humidity, the ions were likely hydrated. The radii of the hydrated ions are in fact in the opposite sequence: Li^+> Na^+> K^+,[24] corresponding to the sequence of activation barriers. Thus, consistency between the simulation and our results is achieved using a model of hydrated ions transported within channels to form capacitive double layers.

3.9 Conclusions

We have investigated ion-incorporated alumina gated ZTO transistors and alumina MIM capacitors with the incorporation of three different alkali metal ions (Li^+, Na^+, K^+). High field-effect mobility (about 20 $cm^2 \cdot V^{-1} \cdot s^{-1}$), high saturation drain current (about 1 mA), and low subthreshold swing (about 200 mV/decade) were achieved in PA- and LA- based FETs operating at 2 V. Therefore, aluminas with the incorporation of three different alkali metal ions (Li^+, Na^+, K^+) act as high-k gate dielectric materials for low-voltage solution-processed oxide FETs. A tendency for ion-incorporated alumina capacitance to increase

with increasing atomic number of alkali metal ions was observed; this could be related to the decrease of alkali ion-oxygen binding strength including decreased hydration numbers. Higher humidity did seem to generally foster increased ion polarization and transport. Increased measurement temperature led to a decrease in both ion-incorporated alumina capacitance and AC conductivity, and the capacitance of lithium incorporated alumina showed the strongest dependence on temperature. Moreover, capacitance of ion-incorporated aluminas with different thickness was measured and capacitance was found to be independent of thickness. With these results, an electric double layer structure was proposed to explain the high capacitance of ion-incorporated alumina dielectrics, and transport of hydrated ions through channels also observed in simulations was proposed to explain ion, frequency, and temperature dependences of capacitance and conductivity.

CHAPTER IV

Ion polarization in alumina under pulsed gate bias stress

4.1 Introduction

Great advances have been made in field-effect transistors (FETs) using oxide semiconductors during the past several years. Compared to traditional silicon semiconductor, oxide semiconductors are promising alternatives in terms of their combined electrical performances, transparency, large area deposition, and mechanical flexibility. Moreover, to reduce power consumption, it is necessary to switch the transistors using low voltage. One means of doing this is to employ the high capacitance generally associated with high-k dielectric materials, meaning oxides such as alumina with higher dielectric constants than that of SiO_2. Incorporation of alkali metal ions in aluminas increases alumina capacitance by more than one order of magnitude at low frequencies.[1-3] Migration of positively charged alkali metal ions in the alumina matrix results in high polarization while a relative high interpore ion transport activation barrier energy inhibits ionic leakage current through the alumina matrix. With solution processing, alumina capacitance can be easily tuned by incorporation of different types of alkali metal ions. With these properties, ion-incorporated alumina becomes a promising gate dielectric material in FETs for low-voltage, solution-processed, and large-area electronics applications.[4]

A well-known drawback of high-k oxide dielectrics, particularly with oxide semiconductors, is the lack of device stability under bias stress, making it important to

understand how the FET threshold voltage (V_{th}) drift occurs. It is now well established that this bias stress is attributed to charge trapping and these traps may be located at the semiconductor/dielectric interface, in the gate dielectric, or within the semiconductor active layer.[5-7] As a consequence, a deterioration of the drain current is recorded, which may be the result of a mobility decrease, subthreshold slope degradation, or a V_{th} shift.[8,9] Although the first bias stress study in an oxide semiconductor was performed in 2006,[10] and despite several attempts to explain this phenomenon, the exact origin and mechanism remain unclear. This bias stress is highly dependent on the involved materials, the device geometry and configuration, the polarization conditions, the gate dielectric and semiconductor deposition temperatures, and the atmosphere in which the device is operating.

Generally, under positive gate voltage stress, n-type amorphous oxide FETs exhibit a positive V_{th} shift, with saturation field-effect mobility and subthreshold slope unchanged. It is widely accepted that the positive ΔV_{th} is caused by electron trapping at the semiconductor-dielectric interface without creating new defects.[5, 11-14] The mobile cations in ion-incorporated aluminas can also create trap sites if they accumulate near the semiconductor interface. Furthermore, by applying gate bias, ion polarization-induced charge trapping can be cumulative if the de-trapping process is slow. Gate pulse techniques are widely applied in transistor stability studies.[15-17] Prompted by the large frequency-dependence of the capacitance and ion mobility in ion-incorporated aluminas that we had observed previously, almost one order of magnitude from 100 Hz to 1 MHz,[3] we were motivated to use pulsed gating to investigate the bias stress mechanisms in this class of dielectrics.

In this study, we examined the dielectric behavior of ion-incorporated alumina in FET structures under pulsed gate bias stress, and characterized the effect of ion polarization over time and at different frequencies on FET transfer curves, finding the effects consistent with dielectric-semiconductor interface charge-trapping activity for the case of Li^+ ions, and defect creation in the case of Na^+ and K^+ ions. The difference in bias stress effect mechanisms among the ions and the generally good stability found for all the ions at the 50 ms time scale are the most prominent findings of this work.

4.2 Experimental Section

Aluminas and ZTO thin films were prepared by sol-gel spin-coating methods. For ion-incorporated aluminas precursor preparation, aluminum nitrate nonahydrate (Sigma Aldrich) and alkali metal salts, such as potassium metabisulfite (Alfa Aesar), sodium bisulfate (Mallinckrodt Chemicals), or lithium acetate dehydrate (Sigma Aldrich), with 11:1 molar ratio were dissolved into 2-methoxyethanol solvent with a molar concentration of 0.5 M. Acetylacetone was then added into the solution with a concentration of 0.5 M. The mixed solution was then stirred at room temperature for 6 hours. Plain alumina precursor solution with a concentration of 0.5 M was also prepared with a similar procedure without adding alkali metal ions. As-prepared precursor solution was kept for 24 hours to promote hydrolysis and filtered through a 0.45 μm PTFE filter.

ZTO solution precursor was prepared by dissolving zinc acetate anhydrous (Alfa Aesar, 0.3 M) and anhydrous tin(II) chloride (Alfa Aesar, 0.3M) in 2-methoxyethanol solution. Acetylacetone (0.6 M) was added into the solution as stabilizer. The mixed solution was

then stirred at room temperature for 12 hours. As-prepared precursor solution was kept for 24 hours to promote hydrolysis and filtered through a 0.45 μm PTFE filter.

For the bottom gate top contact FET fabrication, alumina precursor solution was spin-coated twice onto ITO glass substrate (Delta technologies Ltd., CB-90IN-1105, Display Grade Corning 1737 aluminosilicate glass with about 30 nm ITO coating, RMS roughness of the ITO according to Delta is about 1 nm, measured by Atomic Force Microscope) at 5000 rpm for 30 seconds and then annealed at 300°C for 30 minutes. ZTO precursor solution was then spin-coated onto alumina dielectric film at 3000 rpm for 30 seconds and then annealed in furnace at 500 °C for 1 hour. After annealing, aluminum (100 nm) was deposited by thermal evaporation as source and drain electrodes. Slim-bar TEM grids (SPI Supplies, 200 mesh) were used as a shadow mask and the transistor channel width (W) and length (L) are about 100 μm and 10 μm respectively. The final device layout is shown in Figure S1.

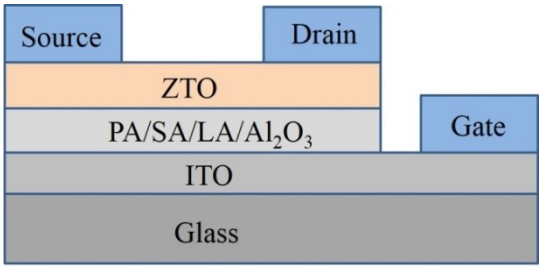
For metal-insulator-metal capacitors, ITO was used as the bottom electrode and thermally evaporated aluminum was used as the top electrode. The dielectric layer was prepared by spin-coating alumina solution twice onto ITO glass substrate (Delta technologies Ltd., CB-90IN-1105, Display Grade Corning 1737 aluminosilicate glass with about 30 nm ITO coating) at 3000 rpm for 30 seconds twice. Between the spin-coatings, as-coated films were prebaked on hotplate at 75 °C for 15 minutes. Final annealing was carried out in a furnace at 500 °C for 1 hour.

Transistor performance was analyzed using an Agilent 4155C semiconductor parameter analyzer. In transfer characteristics measurements, gate voltage wasswept from -5 V to 5

V, with a pulse width of 1 ms and periods of 5 ms, 10 ms, and 50 ms, as illustrated schematically in Figure S2. Drain voltage was kept at 5 V during the measurement. Capacitance of alumina MIM capacitors was measured using an Agilent 4284A precision LCR meter at 100 Hz.

4.3 Effect of pulsed gate bias stress on saturation drain current of ion-incorporated alumina based FETs

To study the pulsed gate bias stress behavior, staggered bottom-gate-oxide FETs were fabricated on 20 nm ITO-coated Corning glass substrates with K^+/$Na^{+/}Li^+$ -incorporated alumina as gate dielectric and zinc tin oxide (ZTO) as the active layer. In a control sample, plain alumina without ion incorporation was used as gate dielectric for a ZTO FET. In pulsed gate transfer characteristic measurements, gate voltages (V_G) with 1 ms "on-state" duration (application time) and different periods (5 ms, 10 ms, and 50 ms) between applications were applied, sweeping V_G from – 5 V to 5 V with a voltage increment of 0.2 V for each sequential V_G application, while keeping drain voltage (V_D) at 5 V. Schematic illustrations of FET structure and pulsed V_G sweep are shown in Figures 4.1. In the "on-state" ($V_G > 0$), electrons in the ZTO layer are attracted to the interface, where they may become trapped, while in the "off-state" ($V_G < 0$), trapped electrons can be released from trap sites. Pulsed gate transfer characteristic measurements were repeated 49 more times with a pause of 15 seconds between each repetition, much longer than the time duration between points of each single sweep.



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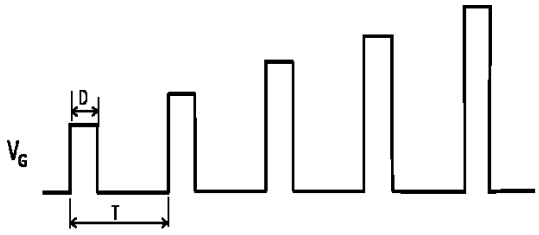
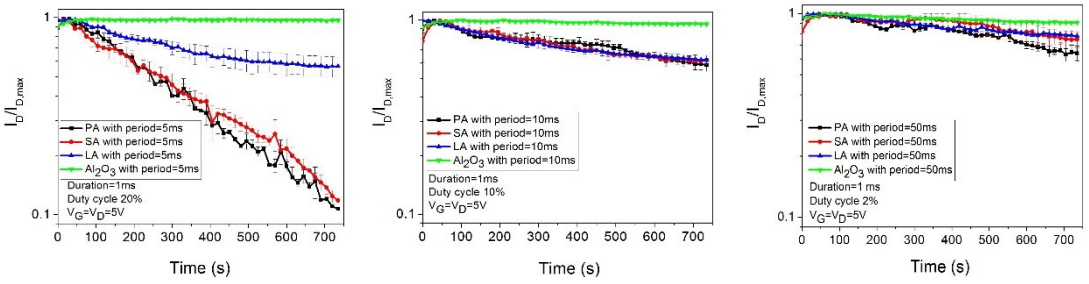


(b)

Figure 4.1 Schematic illustration of (a) ZTO FET with ion-incorporated alumina and plain alumina gate dielectric; (b) pulsed gate "on-state" duration (D) (1 ms) with varied periods (T) (5 ms, 10 ms, and 50 ms). Except for the 1 ms pulse, $V_G = 0$ for the rest of the duty cycle.

The accumulated gate bias stress effect on drain current at a gate-source voltage of 5 V was recorded, and the change in drain current with time duration accumulated over all measurements (including repeated sets of 50 periods of pulsed gate transfer characteristics measurement and 49 pauses of 15 seconds between each pulsed gate transfer characteristics measurement set) is shown in Figure 4.2. Significant differences in the $V_G = 5$ V drain current change were observed with different duty cycles. With a duty cycle of 20%, FETs based on PA and SA gate dielectrics demonstrated the largest decrease of drain current. After 50 measurements, saturation drain current decreased to about 10% of its maximum

value. In comparison, the drain current of LA based FETs decreased about 40% after 50 measurements. Negligible decrease of drain current was seen in FETs with plain alumina gate dielectric. As the duty cycle decreased to 10% (Figure 4.2 (b)), drain current decreased less than 40% in PA and SA FETs; while the magnitude of drain current decrease of LA and plain alumina FETs remains at a similar level as that at 20% duty cycle. The smallest decrease of drain current in ion-incorporated FETs was observed at 2% duty cycle (Figure 4.2 (c)), where there was no significant difference among the aluminas. Figure 4.3 shows the transfer curves shift in ZTO FETs with ion-incorporated alumina and plain alumina gate dielectrics at 20% duty cycle over the time duration of 735 seconds. Before recording series of transfer curves, output curves were obtained as previously published[3] to verify the proper behavior of sample devices.



(a) (b) (c)

Figure 4.2 Pulsed gate bias stress dependence of relative drain current change (on log scale) in ZTO FETs with ion-incorporated alumina and plain alumina gate dielectric. Pulsed gate period: (a) 5 ms; (b) 10 ms; (c) 50 ms. Each point in the plot represents a drain current to max drain current ratio at V_G= 5 V (the last recorded point for each sweep from -5 to 5 V),

with sweeps repeating 50 times during the 735 seconds of the plot. The curves were plotted based on the average of two measurements of every type of sample.

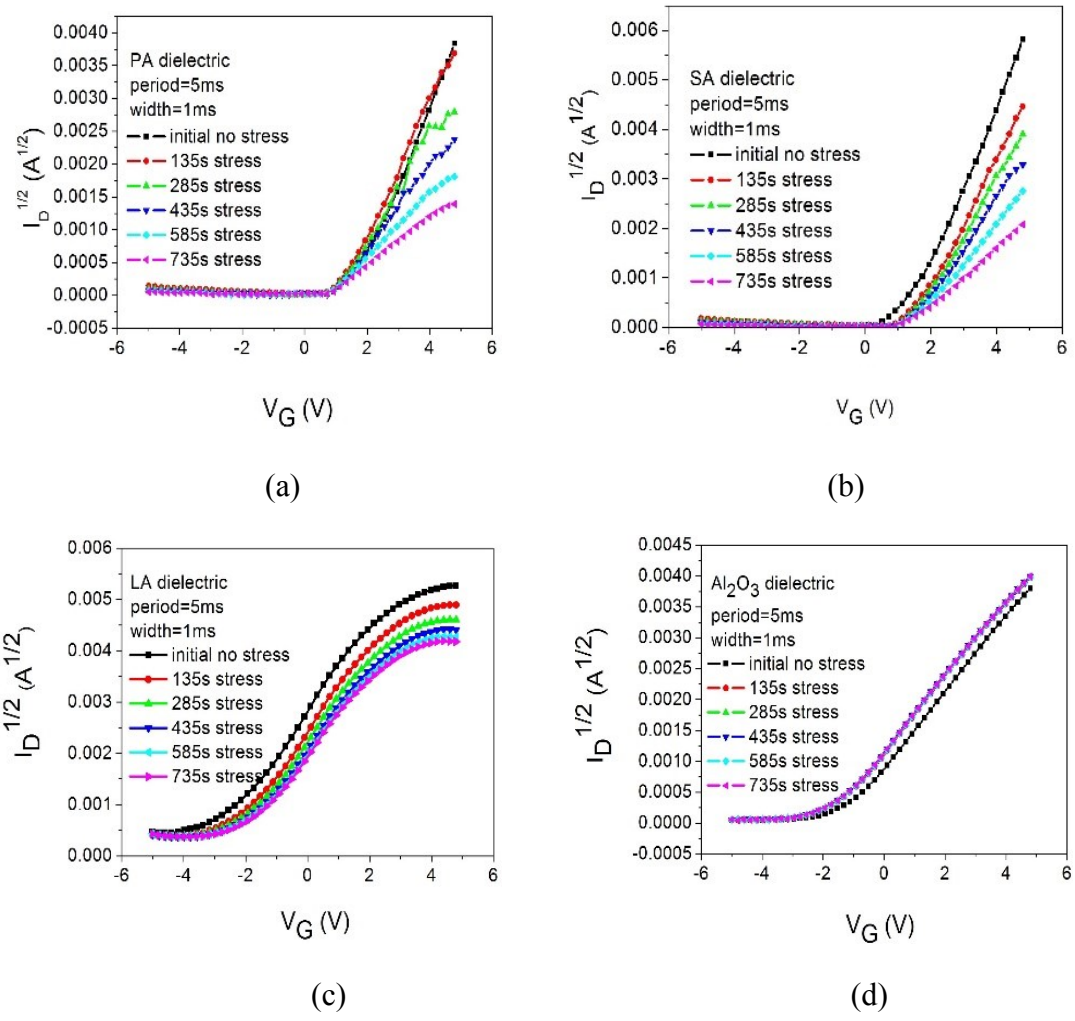


Figure 4.3 Transfer characteristics of ZTO FETs with (a) PA; (b) SA; (c) LA; (d) Al_2O_3 gate dielectrics over the time duration of 735 seconds. Gate voltage duty cycle is 20% (pulse period is 5 ms).

4.4 Effect of pulsed gate bias stress on threshold voltage of ion-incorporated alumina based FETs

According to Equation (1), well established for saturation-regime FETs, a decrease of saturation drain current can be caused by a decrease of saturation field-effect mobility (μ_{sat}), decrease of dielectric capacitance per unit area (C), increase of V_{th}, or a combination of these three factors.

$$I_{D,sat} = \frac{W}{2L}\mu_{sat}C(V_G - V_{th})^2 \tag{4.1}$$

$I_{D,sat}$ is drain current in the saturation regime, and W/L is the width to length ratio.

From the transfer characteristics, threshold voltage (V_{th}) is the intersection between the gate voltage axis and the linear extrapolation of square root of drain current curve. ΔV_{th} is plotted on logarithmic time scales in Figure 4.4 (a), (b), and (c). At all duty cycles, FETs with LA gate dielectric exhibited the largest ΔV_{th} among all samples, even though it showed the smallest current change among the three ion-incorporated aluminas. Most significant ΔV_{th} occurred at a 20% duty cycle. At a 2% duty cycle, the ΔV_{th} of PA and SA FETs are close to zero, while LA still shows a significant shift, though not enough to markedly change the current, as shown in Figure 4.2. The origin of positive ΔV_{th} in amorphous oxide semiconductor FETs is typically attributed to charge trapping in the semiconductor channel and/or at the dielectric/semiconductor interface.[5,11-13] An alternative reason can be back channel exposure to the ambient atmosphere, which induces interaction between active semiconductor layers and moisture.[18] In that study, the measurements were carried out in the open atmosphere that was measured to be at <10% relative humidity, minimizing the impact of moisture on transistor stability. Additional

gate voltage needs to be applied to compensate the electrical field created by the trapped charges; this additional voltage can be quantified by the amount of ΔV_{th}, expressed by

$$\Delta V_{th} = eN_{tr} / C \tag{4.2}$$

where e represents elementary charge, N_{tr} represents surface density of trapped charges, and C represents oxide dielectric capacitance.

Lithium-incorporated alumina exhibited a smaller capacitance (1.8 μF/cm^2 at 100 Hz, relative humidity 30%) than potassium or sodium-incorporated aluminas (2.2 μF/cm^2 at 100 Hz, relative humidity 30%).[3] The large ΔV_{th} of LA samples could be ascribed to its relatively lower capacitance (for a given trap density), or alternatively to the creation of more traps as compared with PA and SA samples. Without strong ion polarization in the gate dielectric, electrons in the channel are less likely to be trapped at the dielectric/channel interface and this explains the smaller ΔV_{th} showed in plain alumina samples in Figure 4.4. In a large duty cycle, alkali metal ions are more frequently pulsed in their alumina matrix and electrons can be embedded more permanently in the channel when V_G is positive. With continuous attractive interaction by migrating positive ions, electrons are more prone to be trapped in interfacial trap states leading to a large ΔV_{th}.

Stretched-exponential time dependence models are widely used to describe threshold voltage shifts in FETs, including amorphous-silicon FETs, amorphous oxide semiconductor FETs, and organic FETs.[19-22] Such models are expressed by the equation

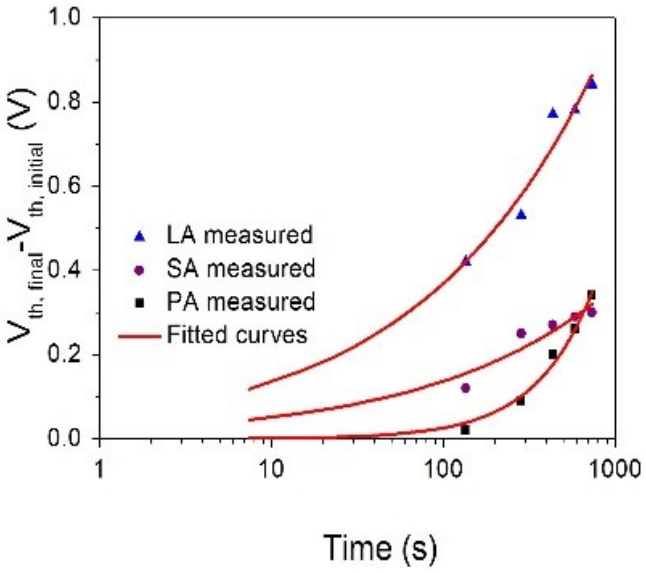
$$\Delta V_{th} = \Delta V_{th0}\{1 - \exp[-(t/\tau)^{\beta}])\} \tag{4.3}$$

Where ΔV_{th0} is ΔV_{th} at infinite time (infinite number of transfer curves) and can be expressed as $\Delta V_{th0} = V_G - V_{th0}$, where V_{th0} is the V_{th} at t = 0. β is a dispersion parameter that

varies slightly with temperature, and τ is a time constant representing the characteristic trapping time of carriers that can be expressed as

$$\tau = \tau_0 \exp(E_T / kT) \tag{4.4}$$

In Equation 4, τ_0 is the thermal prefactor for emission over the barrier,[23] E_T is the average effective energy barrier for electron injection into dielectric/semiconductor interface trap states,[19, 24] and k is the Boltzmann constant. We fit our data, plotted as the time over which pulsed transfer curves are repeated, to this equation as well, realizing that the bias stress voltage is only applied for a fraction of the plotted times. The ΔV_{th} curves fit to the stretched-exponential model are shown in Figure 4.4 and the parameters for fitting are shown in Table 4.1.



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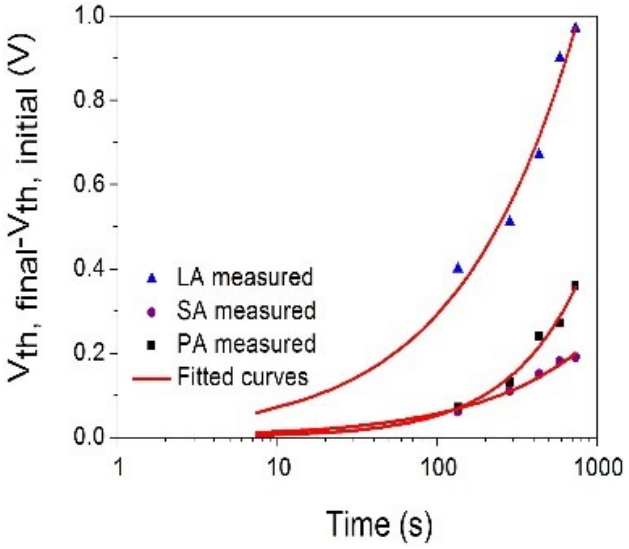

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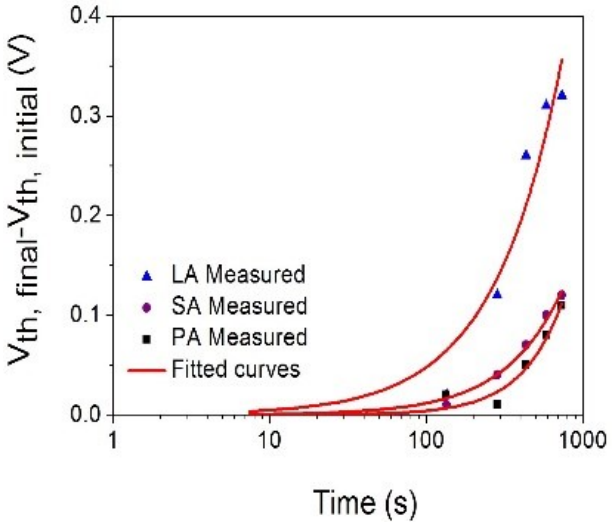


(c)

Figure 4.4 ΔV_{th} vs time plotted in logarithmic scale under gate bias stress of ion-incorporated alumina and plain alumina based ZTO FETs with duty cycle of: (a) 20% (pulsed gate voltage period 5 ms); (b) 10% (pulsed gate voltage period 10 ms; (c) 2% (pulsed gate voltage period 50 ms). Scattered points represent measured ΔV_{th}, red curves show the fitting with stretched-exponential model.

Table 4.1 Stretched-exponential time dependence model fitted V_{th} of ZTO FETs with different gate dielectrics.

Duty cycle		**LA**	**SA**	**PA**
20%	τ (s)	2.2×10^4	4.1×10^4	2.9×10^4
	β	0.61	0.63	0.75
10%	τ (s)	2.2×10^4	5×10^4	5×10^4
	β	0.62	0.7	0.63
2%	τ (s)	2.9×10^4	9.9×10^4	5.8×10^4
	β	0.8	0.76	0.9

For all samples, characteristic carrier trapping times are of the same order of magnitude (10^4 sec, with maximum τ of 9.9×10^4 s), and β varies from 0.6 to 0.9. Similar β and τ values were obtained in other amorphous oxide based FETs. [18, 19-21] According to Equations 3 and 4, a large τ suggests a high stability of V_{th} as well as a small trapped surface charge density. The largest relaxation time of amorphous oxide based transistors is 3×10^5 s, obtained with a magnetron sputtering-fabricated IGZO semiconductor on thermally grown SiO_2 gate dielectric with 200 °C post annealing.[19] Compared with solution processed thin films, high vacuum vapor deposited thin films usually have better quality with less trapping states in interface. The slightly smaller relaxation time observed in our samples could be related to the inevitable surface inhomogeneity of solution-processed thin films compared to vapor-deposited films.

Among ion-incorporated aluminas, LA exhibited the smallest τ, reflecting easier charge injection into dielectric/semiconductor interface trap states. This is consistent with the large ΔV_{th} in LA samples shown in Figure 4.4. For all samples, τ increased with the decrease of duty cycle from 20% to 2%. This result is in accord with less significant ΔV_{th} (greater stability) observed at a small duty cycle.

4.5 Effect of pulsed gate bias stress on capacitance and saturation field-effect mobility of ion-incorporated alumina based FETs

The product of saturation field-effect mobility and capacitance per unit area was also calculated and the change of $\mu C/(\mu C)_{max}$ vs. applied gate bias stress is plotted in Figure 4.5. At a 20% duty cycle, μC of PA and SA samples decreased to about 1/10 of their maximum value after a gate bias stress applied in sweeps over 735 seconds; while a much smaller decrease of μC was exhibited by LA and Al_2O_3 samples. While both parameters decrease, the mobility decreases by a factor of 6-9, while the capacitance decreases by about a factor of 20%-90%, though these decreases may be interdependent because of possible charge density dependence of the mobility. This is a different mechanism of drain current decrease than for LA.

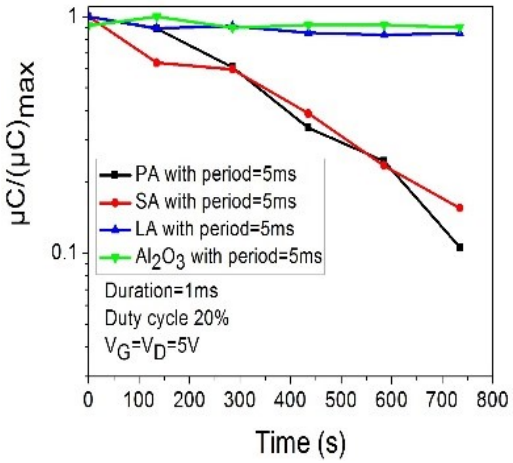
With gate voltage induced nonvolatile polarization, some alkali metal ions could be trapped in the aluminum oxide network. The decreased number of polarizable ions and the repulsion of the mobile ions by those that are trapped would lead to a decrease in dielectric capacitance; fewer ions would approach close enough to the interface to form a molecular-scale double layer. PA has the highest ionic polarizability among the alkali metal ion-

incorporated aluminas considered here, and could therefore have the highest proportion of trapped ions. Therefore, the most significant stress-induced capacitance decrease was observed in potassium-incorporated alumina.

In contrast, at small duty cycles (10% and 2%), the change of μC is insignificant. The change of μC can originate from the change of either field-effect mobility or dielectric capacitance alone, or caused by a combined effect of both. To further investigate μC stability, the effect of gate bias stress on dielectric capacitance was measured based on a MIM capacitor structure using an LCR meter. The capacitance of all the aluminas showed a much smaller gate bias stress dependence compared with μC, with the most significant decrease of capacitance shown in the PA capacitor at 20% duty cycle (Figure 4.6). Thus the decrease of μC with applied gate bias stress can be mainly attributed to a decrease of mobility, and rather than forming localized trap sites, the larger Na^+ and K^+ ions may be affecting the ZTO structure or grain surface chemistry more broadly.

In amorphous silicon transistors, bias stress induced instability is usually caused by two effects: (1) defect creation in the channel layer and (2) charge trapping in the gate dielectric or at the dielectric/channel interface.[7, 25] Amorphous oxide FETs with regular high-k oxide gate dielectrics exhibited positive shifts of V_{th} without significant degradation of mobility under positive gate bias stress.[5, 11] The instability in amorphous oxide FETs is explained by charge trapping at the dielectric/channel interface with little creation of new defect states. The spherical ns orbitals form the carrier conduction band in amorphous oxide semiconductors and the spherically symmetrical nature of the ns orbitals makes them less prone to defect and dangling bond formation.[5] Distinct from regular high-k dielectric-based FETs, oxide FETs with Na^+ or K^+-incorporated alumina gate dielectrics exhibited a

remarkable mobility decrease as bias stress was applied, a sign of the creation of new defect states in the ZTO.



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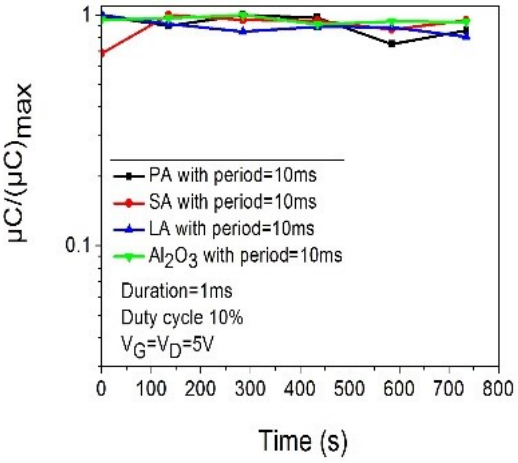

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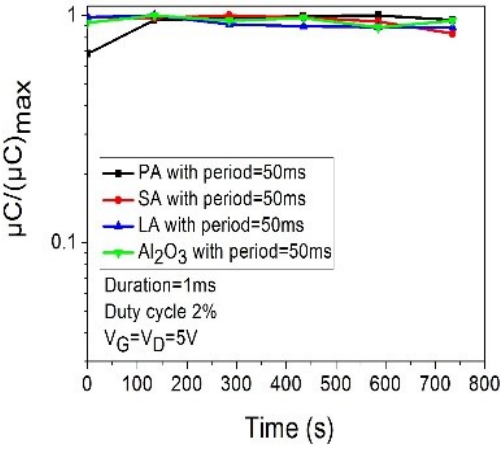

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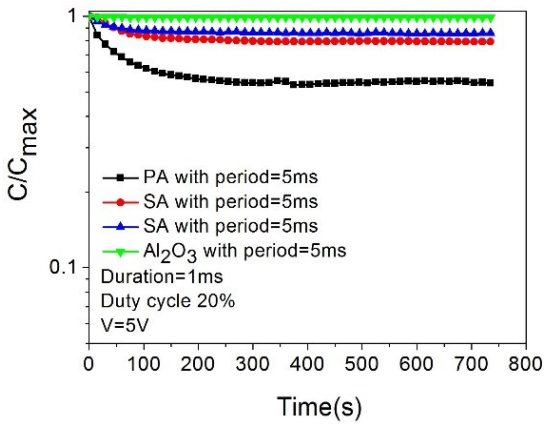
Figure 4.5 Gate bias stress effect on μC of ion-incorporated alumina and plain alumina based ZTO FETs with duty cycle of (a) 20% (pulsed gate voltage duration of 1 ms and period of 5 ms); (b) 10% (pulsed gate voltage duration of 1 ms and period of 10 ms); (c) 2% (pulsed gate voltage duration of 1 ms and period of 50 ms).



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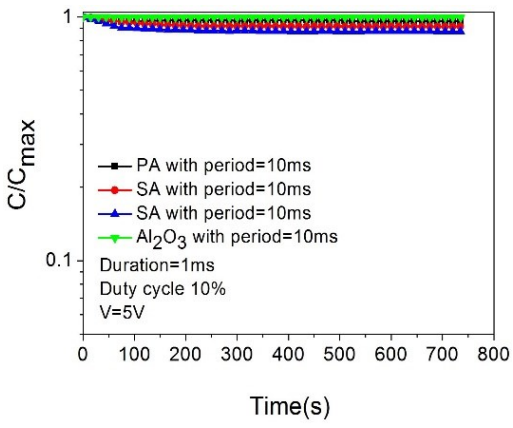

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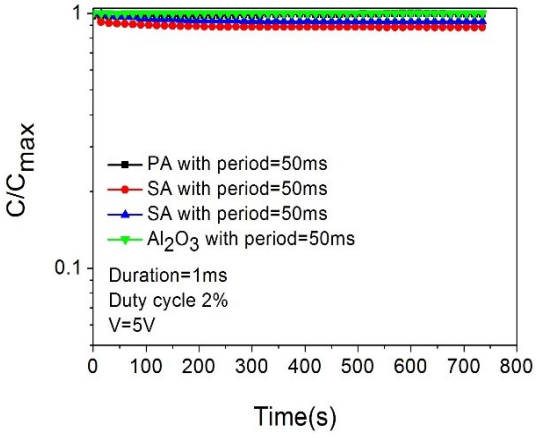

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Figure 4.6 Gate bias stress effect on capacitance of ion-incorporated alumina and plain alumina MIM capacitors with pulsed voltage width of 1 ms and period of: (a) 5 ms; (b) 10 ms; (c) 50 ms.

4.6 Conclusions

In summary, gate bias stress effects on the behavior of ZTO FETs with ion-incorporated alumina and plain alumina were studied. PA and SA FETs exhibited the most significant

drain current decrease with gate bias stress at a 20% duty cycle. Considering the small change in capacitance and V_{th} shown in these samples, the drain current decrease is mainly attributed to the decrease of mobility, possibly caused by new defect states in the ZTO semiconductor. On the other hand, a comparatively larger ΔV_{th} observed in LA samples suggests charge trapping behavior. This result is also supported by the short characteristic trapping time of LA samples obtained by stretched-exponential time dependence model fitting, though the LA current change was also less reversible. Without ion polarization, plain alumina based ZTO FETs exhibited a much smaller drain current change at all duty cycles under gate bias stress, and this result is consistent with the general bias stress behavior of amorphous oxide transistors reported previously. However, provided a duty cycle smaller than 2% is used, the high capacitance of SA and PA can be leveraged with relatively little bias stress instability.

CHAPTER V

Low temperature solution processing of all oxide, low-voltage-operable transparent FETs

5.1 Introduction

Flexible electronics is an emerging area of technology attracting tremendous attention in various applications including displays, photovoltaics, RFID tags, and sensors.[1-5] High-throughput, cost-effective large area processing is critical to expand the application of these technologies with solution processing being viewed as particularly facile. Oxide electronic materials, including both crystalline oxide and amorphous ternary and quaternary complex oxides, can provide useful electrical properties, high chemical and thermal stability, high transparency, and environmentally friendliness. With these properties, oxide semiconductors becomes an ideal substitute for amorphous silicon semiconductor in display application.[6-7] In addition, oxide materials with high dielectric constant and wide band gap are widely used as gate dielectrics in low voltage field-effect transistors (FETs), though many of these are formed at high temperatures.

In flexible electronics applications employing a polymer substrate, low processing temperatures are required to avoid thermal degradation of the substrate. It is a challenge to fabricate a dense impurity-free oxide semiconductor film at a temperature which is lower than the softening temperature of common polymers. To reduce the processing temperature of oxide semiconductors, new types of sol-gel precursors have been designed and new

processing techniques have been used. A water-based ZnO precursor with zinc ammine-hydroxo complex $[Zn(NH_3)_x](OH)_2$ was introduced several years ago to reduce the annealing temperature of zinc oxide (ZnO) thin film.[8] Unlike metal alkoxide sol-gel precursors with organic solvents, aqueous solution precursors decompose at low temperature (< 150 °C) and leave much less residue in the oxide thin films after annealing, and thus are favorable for achieving high thin film uniformity and good charge transport properties. Based on this precursor, ZnO based FETs exhibited a saturation field-effect mobility at 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$ after 200 °C post-annealing in nitrogen.[8] However, repeated time-consuming centrifugation and decantation steps are required to remove Na^+ and NO_3^- ions from the precursor. Another approach for low temperature solidification of oxide thin films harnesses the rapidly release of energy resulting from a localized exothermic redox reaction ignited by a low annealing temperature.[9-11] The reaction was generated with the participation of oxidizer and fuel. Acetylacetone or urea were used as a 'fuel' and metal nitrates were used as oxidizers.

Recently, a self-combustion precursor was introduced to improve the combustion efficiency. With this precursor, a high-k AlO_x gate dielectric with low leakage current was fabricated at a relatively low temperature of 250 °C.[12] 'Sol-gel on chip' processes have been designed to create high performance solution-processed oxide thin films below 250 °C.[13] In this method, hydrolysis occurs on the surface of the film during spin-coating, and thus avoids the undesired precipitation and particle growth steps which would affect the electrical properties of oxide semiconductors. However, this is a less convenient processing procedure because it needs to be carried out in an inert atmosphere to avoid undesirable precursor hydrolysis. Oxide thin film processing temperature can also be reduced with the

assistance of deep-ultraviolet (DUV) light. DUV light facilitated condensation and densification of sol-gel processed thin films by photochemical cleavage and rearrangement of M-O-M networks, where M indicates the metal ions of the oxide semiconductor.[14-16] Using both high energy DUV light and moderate annealing temperature (about 150 °C), indium zinc oxide (IZO), indium gallium zinc oxide (IGZO), and indium oxide (In_2O_3) based FETs exhibited excellent transistor performance.[14]

Amorphous metal oxides composed of heavy metal cations with an electronic configuration $(n-l)d^{10}ns^0$, with $n \geq 4$, demonstrate high electron mobility and thus become promising candidates to supersede a-Si:H in large-area FETs.[13-15] In these amorphous metal oxides, the bottom part of the conduction band is composed of a linear combination of n s orbitals. The large overlap of n s orbitals with spherical symmetry results in high mobility.[13-15] Indium-based amorphous oxides, such as IZO and IGZO, exhibit good electrical properties even with low temperature processing.[9,11] However, a looming shortage of indium would inhibit the employment of indium-based oxides in large-area electronics.

To simplify aqueous ZnO precursor processing steps, we have developed a new preparation strategy without centrifugation and decantation steps. This processing route consists of two steps: First, dissolution of zinc nitrate hexahydrate and acetylacetone in ammonium hydroxide stirring vigorously at room temperature for 20 h, and second, dilution with ultrapure water (UPW). The resulting solution can then be spin-coated. The zinc tin oxide (ZTO) amorphous semiconductor layers created in this way have excellent FET electron transport properties. Tin (II) fluoride has good solubility in water and was chosen as tin source for the aqueous ZTO precursor.[16,17]

In portable and flexible electronics applications, low temperature processing of high-k dielectrics is also needed to reduce FET operation voltage. In our previous research, sol-gel solution processed alkali metal ion-incorporated aluminas demonstrated very high capacitance with small leakage current and thus became a good candidate for low voltage FETs.[18-20] Due to the difference in ion-oxygen binding strength, the capacitance of alumina could be tuned by incorporating alkali metal ions with different atomic numbers. In this paper, two types of sodium-incorporated alumina (SA) combustion precursors were synthesized and spin-coated as the gate dielectric of low temperature processed ZnO FETs. In the first precursor, aluminum nitrate was used as the oxidizer and urea was used as fuel. A self-combustion SA precursor was also prepared with aluminum nitrate and aluminum acetylacetonate as oxidizer and fuel, respectively. To improve SA film morphology, (3-glycidoxypropyl) trimethoxysilane (GPTMS) was added in the self-combustion precursor as a binding agent to cross-link the aluminum oxide matrix. In contrast to other types of silanes, blending GPTMS in SA precursor did not change the hydrophilic nature of the SA thin film surface, and this could be related to the formation of polar functional groups as the epoxy groups open during curing. The high dielectric constant of GPTMS is also beneficial in maintaining the high capacitance of the SA dielectric.

5.2 Experimental section

Low temperature aqueous ZnO precursor was prepared by dissolving zinc nitrate hexahydrate (Sigma Aldrich) in ammonium hydroxide (Fisher) with a zinc concentration of 0.6 M. Acetylacetone (0.2M) (Sigma Aldrich) was added as stabilizer. After stirring at room temperature for 30 hours, the precursor solution was filtered through a 0.45 μm PVDF

filter and then diluted with ultrapure water (UPW) with a UPW to precursor volume ratio 4:1, ready for spin-coating ZnO thin films.

To prepare low temperature ZTO precursor, zinc nitrate hexahydrate (Sigma Aldrich) and tin (II) fluoride (Sigma Aldrich) were dissolved in ammonium hydroxide (Fisher) with a 1:1 molar ratio to make a total precursor concentration of 0.6 M. 0.2 M acetylacetone (Sigma Aldrich) was the added to the precursor. After stirring at room temperature for 30 hours, the precursor solution was filtered through a 0.45 μm PVDF filter and then diluted with ultrapure water (UPW) with a UPW to precursor volume ratio 4:1.

In urea-based combustion SA precursor preparation, aluminum nitrate nonahydrate (Sigma Aldrich) and sodium bisulfate (Mallinckrodt Chemicals) were dissolved in 2-methoxyethanol (Sigma Aldrich) with Al^{3+} to Na^{+} molar ratio of 11:1. The total concentration of the precursor is 0.3 M. 0.15 M urea (Sigma Aldrich) was added as fuel for combustion reaction. 0.3 M acetylacetone (Sigma Aldrich) was added as stabilizer. The mixed solution was then stirred at room temperature for 6 hours and kept for 24 hours to promote hydrolysis and filtered through a 0.45 μm PTFE filter before spin-coating.

In preparing self-combustion SA precursor, aluminum nitrate nonahydrate (Sigma Aldrich) and aluminum acetylacetonate (Sigma Aldrich) with equivalent molar amounts were dissolved in 2-methoxyethanol (Sigma Aldrich) to make solution with a concentration of 0.3 M. Sodium bisulfate (Mallinckrodt Chemicals) was added in the precursor with Al^{3+} to Na^{+} molar ratio of 11:1. (3-glycidoxypropyl) trimethoxysilane (GPTMS) (Sigma Aldrich) was added in the precursor solution with an Al^{3+} to GPTMS molar ratio of 10:1 and 2:1.

After stirring at room temperature for 6 hours the precursor was kept for 24 hours and filtered through a 0.45 μm PTFE filter before spin-coating.

SA MIM capacitors were fabricated by spin-coating combustion SA precursors twice on ITO glass substrate (Delta technologies Ltd., CB-90IN-1105, Display grade Corning 1737 aluminosilicate glass with about 30 nm ITO coating, RMS roughness of the ITO is about 1 nm) at 3000 rpm for 30 seconds. After spin-coating for the first time, as-coated films were pre-baked on a hot plate at 75 °C for 15 min. For urea-based precursor processed SA the final annealing was carried out on hot plate at 200 °C for 6 hours. For self-annealing precursor processed SA, the films were finally annealed at 250 °C for 6 hours. 100 nm aluminum was thermally evaporated on SA film as the top electrode of the MIM capacitor.

For XRR analysis, both urea-based combustion precursor and self-combustion precursors were used to deposit SA films on HF-etched silicon substrates. After initial spin-coating, SA films were pre-baked on a hot plate at 75 °C for 15 minutes. This process was then repeated 1 to 3 times and SA films were annealed in a furnace at 500 °C for 1 hour. In some samples, aqueous ZnO precursor was spin-coated on annealed SA films for 1 time and finally annealed in a furnace at 500 °C for 1 hour.

For low temperature processed ZnO and ZTO FETs, precursors were spin-coated once on heavily n-type doped Si substrate with 300 nm SiO_2 at 3000 rpm, 30 seconds. As deposited films were annealed on a hot plate at 200 °C or 250 °C for 1 hour. After that, aluminum (100 nm) was deposited by thermal evaporation as source and drain electrodes. A Slim-bar TEM grid (SPI Supplies, 200 mesh) was used as shadow mask, with typical channel width (W) of 100 μm and channel length (L) of 10 μm.

To fabricate low temperature low voltage field-effect transistors, combustion SA precursors were spin-coated twice (3000 rpm, 30 seconds) on ITO glass substrates and annealed at 200 °C (for urea based precursor) or 250 °C (for self-combustion precursor) for 6 hours. To pattern ZnO layer, a 1 cm×1 cm square was drawn with Novec (3M) on an SA film before ZnO deposition. Aqueous ZnO precursor was then dropped into the Novec boundary and spin-coated once on the SA film at 3000 rpm, 30 seconds and annealed on hotplate at 200 °C for 12 hours. Aluminum (100 nm) was evaporated as source and drain electrodes with slim-bar TEM grid (SPI Supplies, 200 mesh) as shadow mask.

XRD analysis was carried out with Philips X'Pert Pro X-ray Diffraction System.

XPS spectrum and thin film surface atomic concentration were measured by PHI 5600 X-ray photoelectron spectrometer. Thermal properties of thin film were measured by DSC (TA Instruments Q20). Thin film surface roughness was measured by AFM (VeecoMultiMode with NanoScopeIIIa controller) with a tapping-mode at a scanning frequency of 0.25 Hz. Root-mean-square (rms) values were obtained by scanning a 2μm ×2μm surface area.

Transistor performance and leakage current of MIM capacitors were analyzed with an Agilent 4155C semiconductor parameter analyzer. Capacitance of MIM capacitors was measured with an Agilent 4284A LCR meter.

X-ray reflectivity data were collected using a Panalytical X'Pert MRD using CuKα x-ray radiation. X-ray reflectivity data were fit using the interdiff model of the GenX software. The fits were obtained by fitting the layer thicknesses, electron densities, and interfacial roughnesses and minimizing the differences between the data and the model reflectivity

curve. Geometric factors such as sample and beam size were taken into account, but not fit. A series of layers consisting of a silicon substrate, a sublayer between silicon and SA layer, a SA layer, and a ZnO top layer was used to model the sample structure.

5.3 200 °C processing of aqueous ZnO and ZTO based FETs on SiO_2 gate dielectric

A 200 °C-annealed ZnO thin film showed excellent crystallinity with a sharp (002) peak in the x-ray diffraction pattern in Figure 5.1. The x-ray diffraction pattern shows that the ZnO layer has a wurtzite crystal structure with preferred growth along the c-axis. ZTO thin films annealed at 200 °C and 250 °C are, however, lack well-defined x-ray reflections and are apparently amorphous.

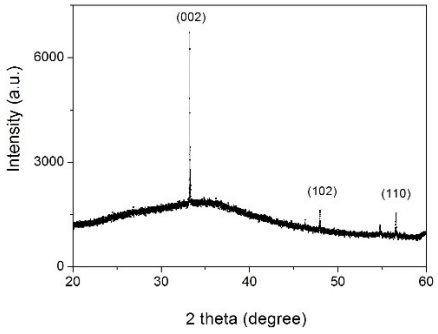
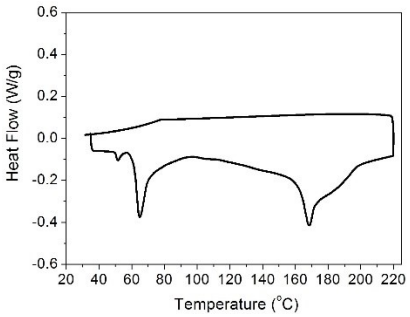
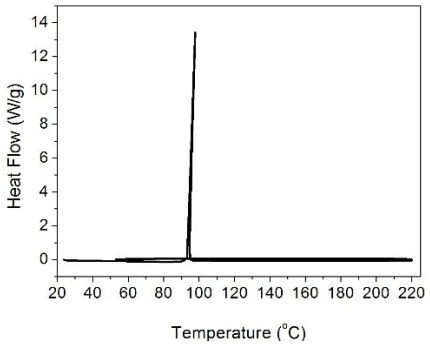


Figure 5.1 X-ray diffraction pattern of ZnO thin film annealed at 200 °C for 1 hour.



(a)



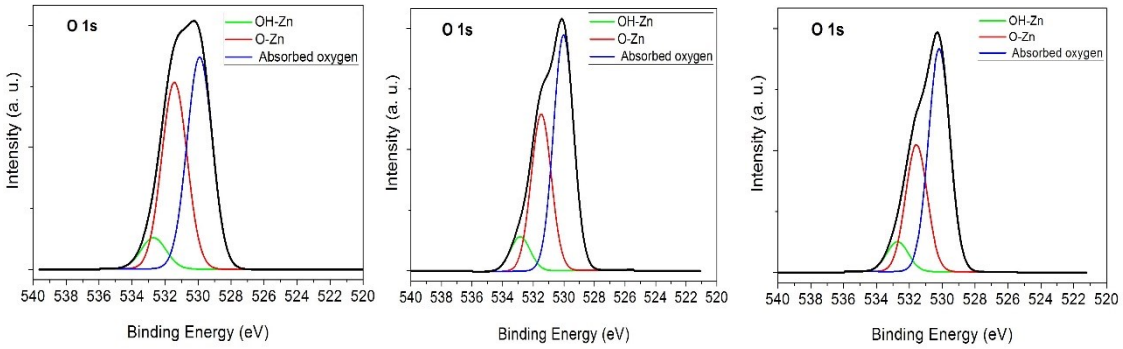
(b)

Figure 5.2 DSC spectrum of aqueous (a) ZnO precursor; (b) ZTO precursor.

The thermal properties of the aqueous ZnO and ZTO precursors were analyzed by differential scanning calorimetry (DSC), as shown in Figure 5.2. In the ZnO sample, two main steps for zinc ammine-hydroxo complex decomposition are represented by two endothermic reaction peaks located at 65 °C and 170 °C. The small endothermic peak at 45 °C could be attributed to the removal of excess ammonium hydroxide from sample. No peaks were observed in the region between 170 °C and 220 °C. This suggests a complete conversion from ammine-hydroxo precursor to solid ZnO thin film at a temperature lower than 200 °C. A similar thermal behavior was reported in ZnO prepared with an aqueous precursor by dissolving zinc chloride in aqueous ammonia.[21]

In contrast to the ZnO sample, a strong exothermic reaction occurred at a temperature less than 100 °C in the ZTO sample, representing ZTO formation below 100 °C (shown in Figure 5.2 (b)). This significant amount of energy released from the strong exothermic reaction would be attributed to the redox reaction of $Zn(NO_3)_2$ and SnF_2. A similar exothermic reaction peak was observed in a combustion ZTO precursor around 100 °C analyzed by differential thermal analysis (DTA).[9]

The chemical compositions of ZnO and ZTO thin films were characterized by XPS. Figure 5.3 shows the O 1s spectrum of ZnO and ZTO samples annealed at different temperatures. The O 1s peak could in each case be deconvoluted into three subpeaks at 530.0±0.1 eV, 531.5±0.1 eV, and 532.7±0.1 eV. For both ZnO and ZTO samples, the subpeak at 530.0±0.1 eV has the highest intensity. This subpeak can be attributed to the M-O-M lattice.[22] A higher M-O-M lattice subpeak intensity in Figure 5.3 suggests a more complete transformation from aqueous precursors to solid ZnO/ZTO films. Subpeaks at 531.5±0.1 eV and 532.7±0.1 eV are related to metal hydroxide (M-OH) components and weakly bonded (M-OR) components.[11] Comparing Figure 5.3 (b) and (c), the ZTO thin film annealed at 300 °C showed an attenuated M-OH subpeak, which represents a more complete transition from precursor solution to solid Zn-O-Sn lattice structure with a higher annealing temperature.



(a) (b) (c)

Figure 5.3 O 1s XPS spectrum of (a) ZnO annealed at 200 °C for 1 hour; (b) ZTO annealed at 200 °C for 1 hour; (c) ZTO annealed at 300 °C for 1 hour.

Figure 5.4 shows the SEM image of ZnO thin film spin-coated on ITO glass substrate. A dense and homogeneous ZnO surface with well-connected grains as shown in the image

is critical for achieving high electron mobility in ZnO thin films and good performance in ZnO FETs.

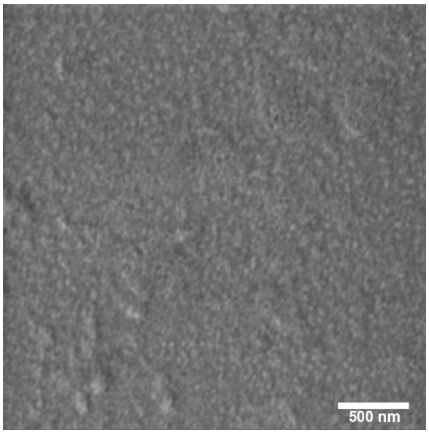


Figure 5.4 SEM image of ZnO annealed at 200 °C for 1 hour.

The fabrication process for low-processing temperature ZnO FETs followed a series of steps. First, the as-prepared ZnO precursor was spin-coated one time on heavily an n-type doped silicon substrate with 300 nm SiO_2 as gate dielectric and then annealed at 200 °C for one hour. The schematic of a ZnO FET is shown in Figure 5.5. A ZnO film made under similar conditions on a bare silicon wafer had a thickness of about 6±1 nm as characterized by XRR, as shown in Figure 5.6.

Figure 5.7 exhibits representative output and transfer characteristics of ZnO FETs. The drain current demonstrates a good modulation behavior induced by gate voltage in output characteristics. Based on the analysis of over 30 samples, the saturation field-effect mobility was 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$. A representative transfer curve shown in Figure 5.7 (b). The on/off current ratio was 6.2×10^4. The threshold voltage was 5 V, and the subthreshold slope was 5.7 V/decade.

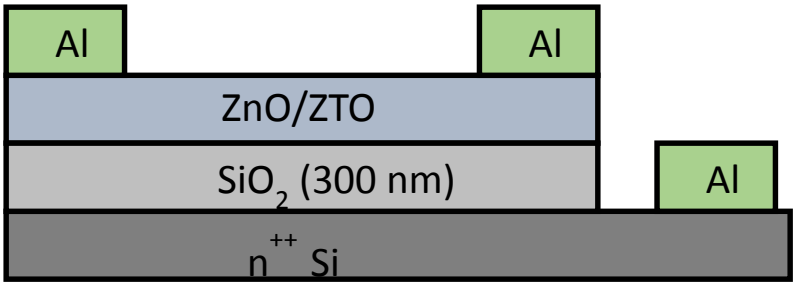


Figure 5.5 Schematic of a ZnO/ZTO based FET configuration.

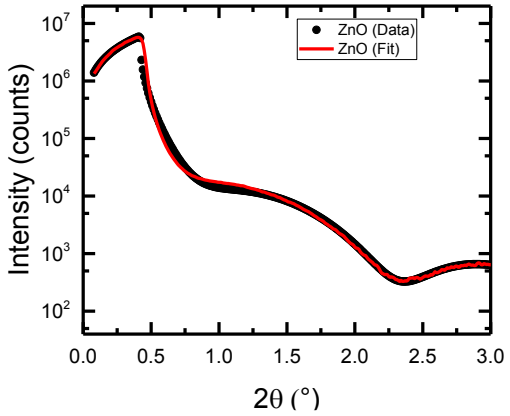
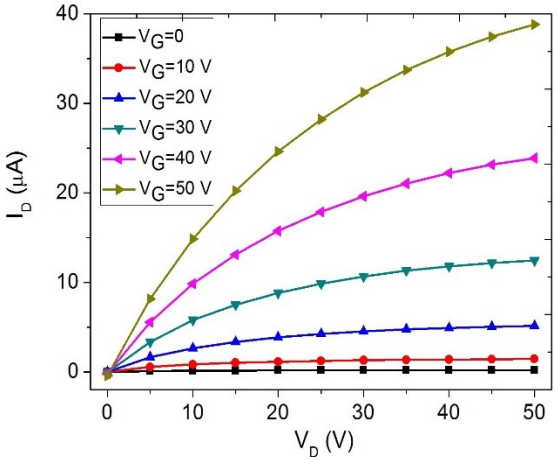
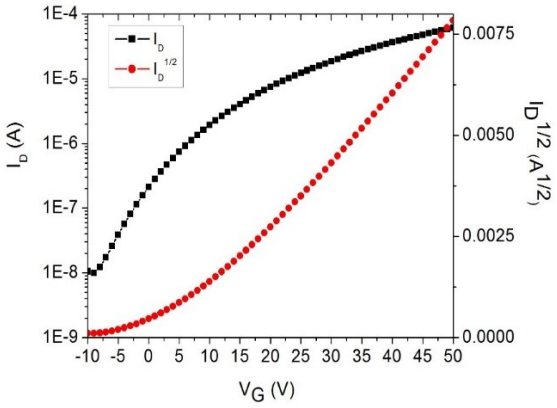


Figure 5.6 X-ray reflectivity data from a ZnO film deposited on a Si wafer. A film thickness of 6±1 nm was determined from the fit.



(a)



(b)

Figure 5.7 (a) Output and (b) transfer characteristics of ZnO based FETs with 300 nm SiO_2 gate dielectric annealed at 200 °C for 1 hour.

Low temperature ZTO-based FETs were also fabricated by spin-coat processing with 300 nm SiO_2 as gate dielectric. Figure 5.8 shows the transistor performance of ZTO FETs processed at 200 °C and 250 °C. At the higher annealing temperature of 250 °C, the on-off current ratio increased more than two orders of magnitude. This increase reflects a significant improvement of ZTO film quality and/or a reduced concentration of defects or impurities at the SiO_2/ZTO interface. Low temperature processed ZTO FETs shown in Figure 5.8 exhibited a similar saturation field-effect mobility as ZnO FETs fabricated at 200 °C in Figure 5.7. Detailed transistor parameters of ZTO FETs are shown in Table 5.1.

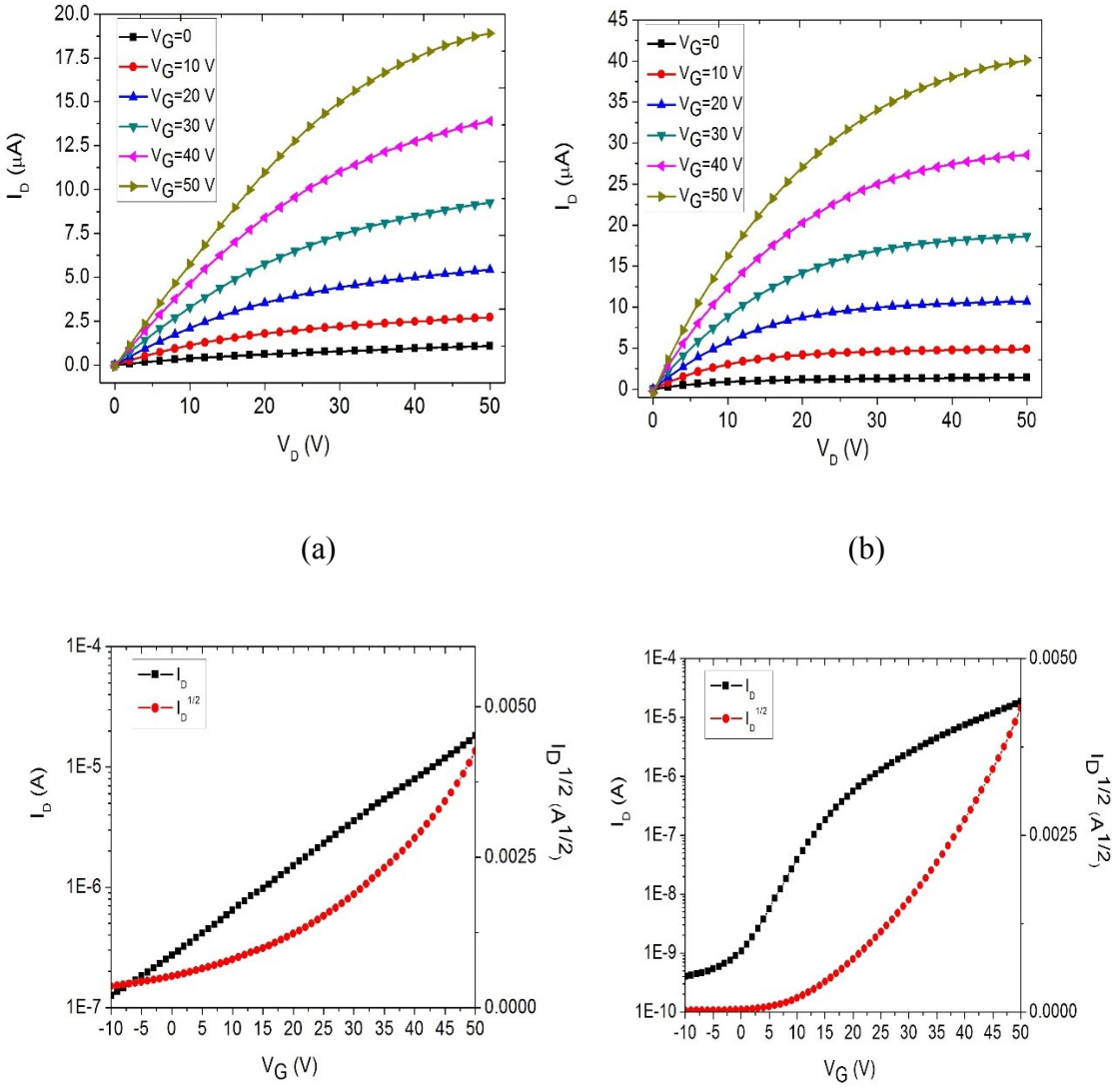


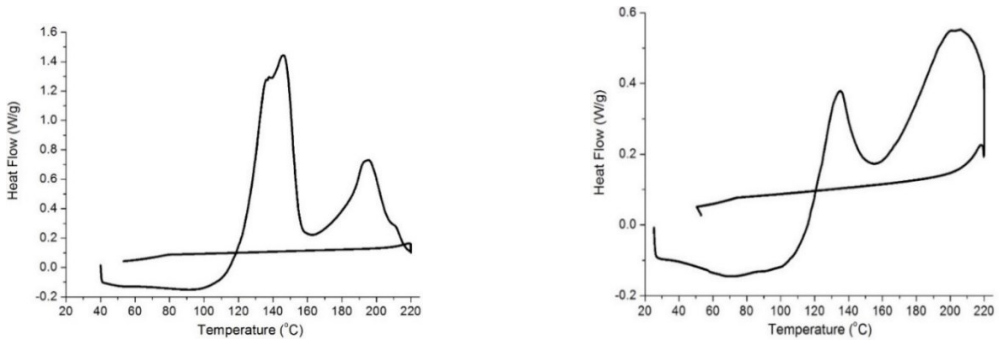
Figure 5.8 Transistor performance of ZTO FETs with SiO_2 gate dielectric. Output characteristics with (a) 200°C, and (b) 250 °C annealing. Transfer characteristics with (c) 200 °C, and (d) 250 °C annealing.

Table 5.1 Typical transfer characteristics of ZTO based FETs with 300 nm SiO_2 gate dielectric.

Processing Temperature (°C)	W/L	V_{th}(V)	μ_{sat} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	I_{on}/I_{off}
200 °C	10	19	0.7	144
250 °C	10	17	0.7	4.6×10^4

5.4 Low temperature processing of combustion SA dielectric in FETs application

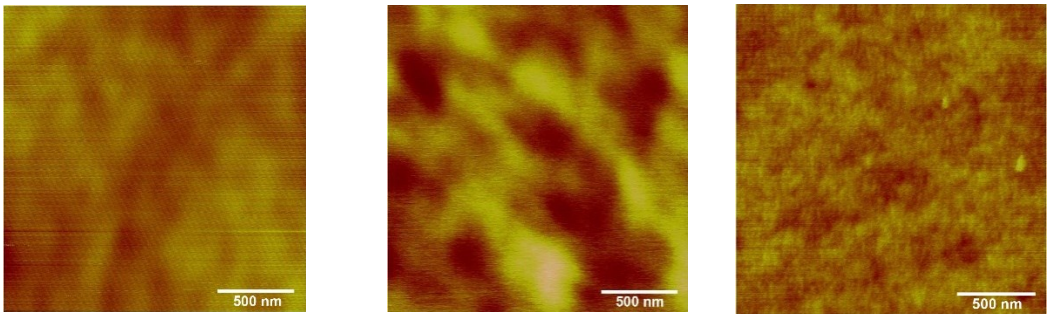
Thermal analysis was carried out to analyze the redox exothermic reaction in the combustion SA precursors. Two exothermic reaction peaks at about 140 °C and 190 °C were observed in the urea-based SA precursor as shown in Figure 5.9 (a). This result corresponds to a two-step precursor conversion below 200 °C with a major conversion at 140 °C. In our urea-based combustion SA precursor, the exothermic reaction occurred at a lower temperature than that in Al_2O_3 combustion precursor with urea fuel reported before.[12] Similar to the urea-based combustion SA precursor, two exothermic reaction peaks at 135 °C and 200 °C were observed in the self-combustion precursor SA sample. Compared with the urea-based precursor, a major exothermic reaction occurred at a higher temperature (200 °C) in the self-combustion precursor sample, suggesting a slightly higher decomposition temperature.



(a) (b)

Figure 5.9 DSC scan of SA precursors (a) urea based; (b) self-combustion precursor.

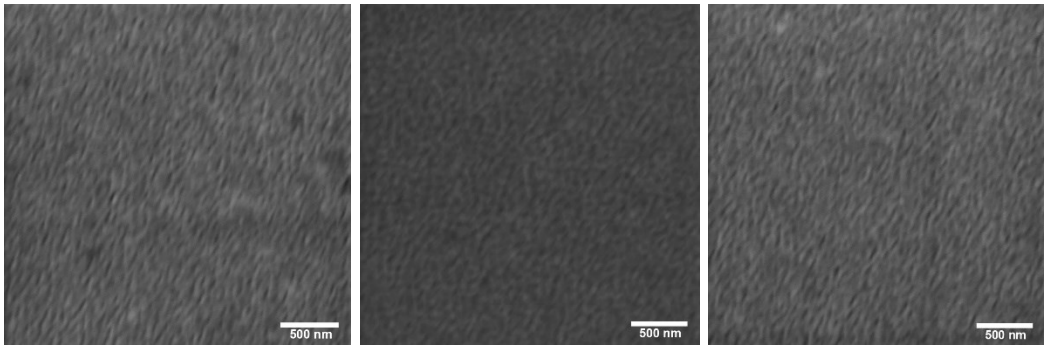
Surface morphology of combustion processed SA thin films were analyzed by atomic force microscopy (AFM), as shown in Figure 5.10. The root-mean-square roughness self-combustion precursor processed SA decreased from 0.46 nm to 0.20 nm as the amount of GPTMS was increased from 10 at% to 50 at%. A smaller roughness, 0.17 nm, was obtained in an SA film prepared with urea-based combustion precursor. This smooth SA surface facilitates ZnO nucleation and growth on top to achieve preferred electrical properties.



(a) (b) (c)

Figure 5.10 AFM image of SA thin films prepared by (a) urea-based combustion precursor; (b) self-combustion precursor with 10 at% GPTMS; (c) self-combustion precursor with 50 at% GPTMS.

According to SEM images shown in Figure 5.11, combustion processed SA films exhibited dense and uniform surfaces. A dense and homogeneous film is required to reduce leakage current though the dielectric film.

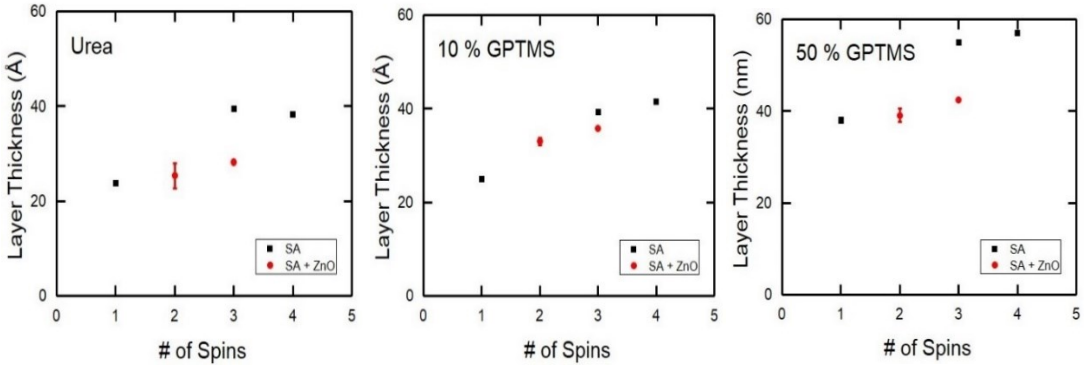


(a) (b) (c)

Figure 5.11 SEM image of SA thin films prepared by (a) urea based combustion precursor; (b) self-combustion precursor with 10 at% GPTMS; (c) self-combustion precursor with 50 at% GPTMS.

The three different SA compositions shown in Figure 5.11 were also characterized by XRR. The main goal of the reflectivity experiments was to measure the thickness of the oxide layer deposited in each step. With this goal in mind, a final anneal at 500°C was performed prior to the x-ray reflectivity analysis to eliminate any possibility of solvent contributions to the thicknesses. The initial spin-coating of the urea-based, 10% GPTMS, and 50% GPTMS materials gave layers that were 24, 25, and 38 nm thick, respectively. Subsequent coatings yielded additional thickness, but not the same increments as from the first layer. Figure 5.12 (a), (b), (c) show the thickness increases with the number of spin-coatings. In these figures, the black points are SA only, while the red points are from films that were capped with ZnO, as would be done for FETs. It can be seen that the application

of a ZnO layer results in the apparent etching of some SA film by about 10 nm, even as a ZnO layer is also formed, as is made clear by the FET characterizations to be discussed below. Roughnesses determined by XRR are consistent with those observed by microscopy.

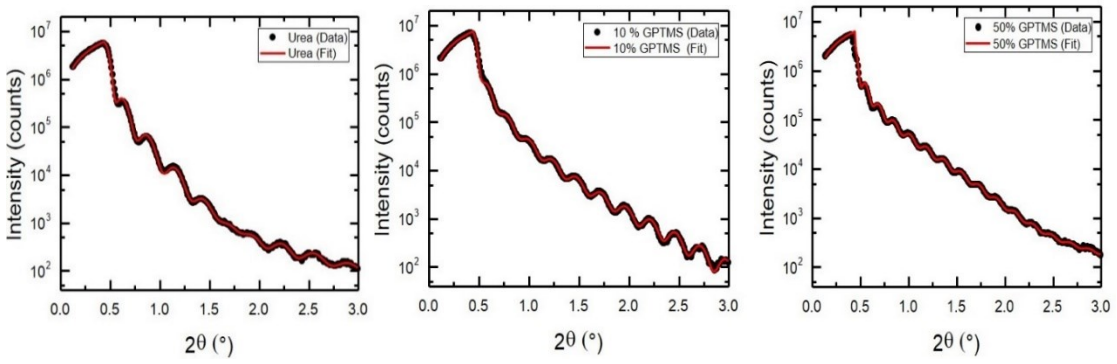


(a) (b) (c)

Figure 5.12 Plots of SA layer thickness vs. number of spin coatings for (a) urea, (b) 10% GPTMS, and (c) 50% GPTMS precursors. The black dots are measurements from samples without a ZnO top layer and the red dots are measurements from samples with a ZnO top layer. The thickness of the SA layer does not increase linearly with the number of spins. Additionally, it can be seen that the application of the ZnO layer etches the underlying SA layer, while still forming the ZnO top layer.

Representative XRR data are shown in Figure 5.13. Annealing of SA films at 500 °C for 1 hour seems to create a sublayer of different electron density at the silicon-SA interface. The average thickness of this sublayer across all fits in the samples is 5.3 nm ± 1.7 nm. It is unclear if the thickness of the new sublayer depends on the precursor solution or not. The magnitudes of the sublayer electron density values differ from their SA counterparts by an average of 3-6% across all precursors. However, fits to the XRR data are equivalently

good whether the sublayer electron density value is assumed to be both higher and lower than the corresponding SA layer, making it unclear if the sublayer is more or less electron rich than its SA counterpart.

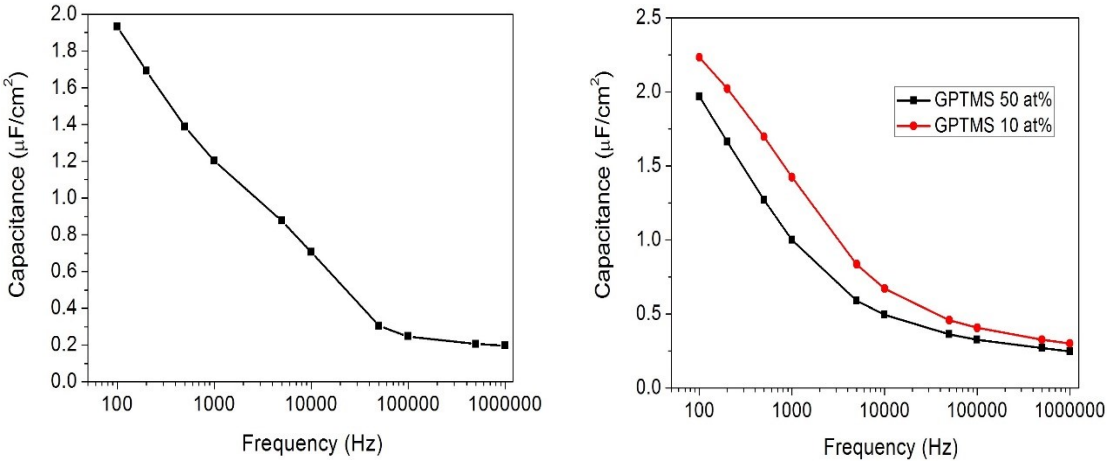


(a) (b) (c)

Figures 5.13 X-ray reflectivity data from (a) urea, (b) 10% GPTMS, and (c) 50% GPTMS. The data are fit by GenX using the interdiff model.[23] The model fits layer thickness and electron density and the root-mean-square roughness of the interface between the layers.

The frequency dependence of capacitance of SA MIM capacitors prepared with both urea based combustion precursor and self-combustion precursor is shown in Figure 5.14. For both types of SA MIM capacitors, capacitance decreases with the increase of frequency, leveling at a capacitance similar to that of plain aluminum oxide (without sodium ion-incorporation) in the high frequency region. The high capacitance observed at low frequency could be attributed to electric double layer formation caused by the polarization of alkali metal ions. This capacitance behavior is similar to that of a SA MIM capacitor fabricated at 500 °C with a conventional SA precursor.[20] As shown in Figure 5.14 (b), the increased amount of GPTMS in SA led to a modest decrease in SA dielectric capacitance. However, polymerization of GPTMS and cross-linking with aluminum oxide did not

greatly affect the polarization of sodium ions in aluminum oxide matrix as a high capacitance is observed in the low frequency region.

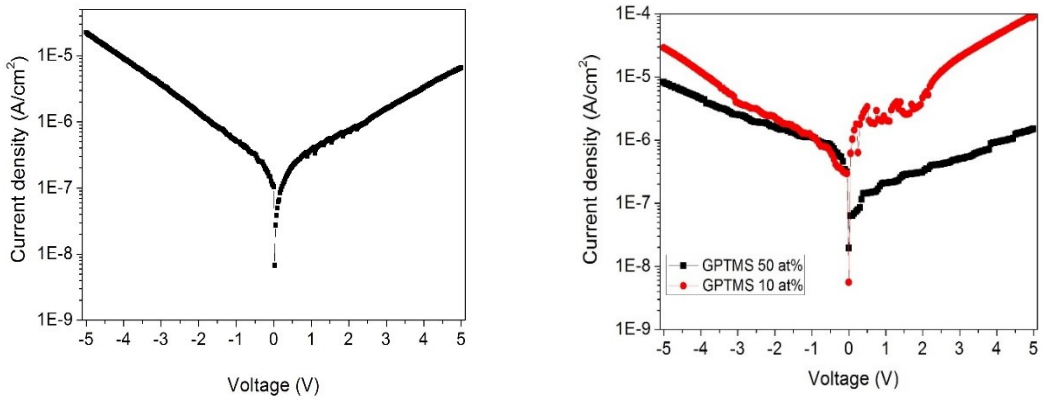


(a) (b)

Figure 5.14 Frequency dependence of capacitance of (a) urea based combustion precursor prepared SA MIM capacitor and (b) self-combustion precursor prepared SA MIM capacitors with 10 at% and 50 at% GPTMS from 100 Hz to 1 MHz.

Generally speaking, it is a challenge to obtain low leakage current in solution- processed dielectrics annealed at low temperature. Incomplete decomposition of precursor solution and/or formation of porous structure during low temperature annealing provide charge transport channels and/or breakdown sites, and lead to high leakage current. As shown in Figure 5.15, low leakage current was achieved in both types of SA MIM capacitors between -5 V to 5 V. Leakage current of all SA samples were of the same order of magnitude as the leakage current of 500 °C annealed SA MIM capacitors reported before.[20] Comparing Figure 5.15 (a) and (b), self-combustion SA MIM capacitors exhibited a lower leakage current than urea-based combustion precursor processed SA capacitors. Supported

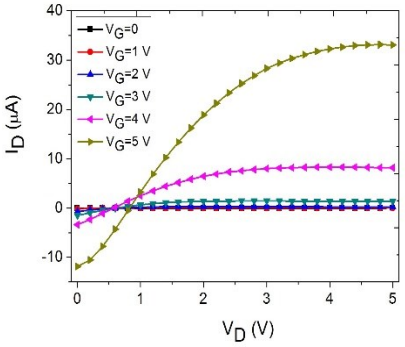
by surface morphology data shown previously, this could be related to denser film structure in the self-combustion SA film with the incorporation of GPTMS. As expected, leakage current decreased significantly by increasing the amount of GPTMS from 10 at% to 50 at%, especially in the positive voltage region.



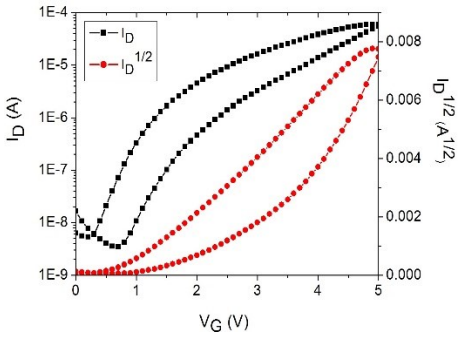
(a) (b)

Figure 5.15 Leakage current of SA thin film prepared by(a) urea based combustion precursor; (b) self-combustion precursor with 10 at% and 50 at% GPTMS.

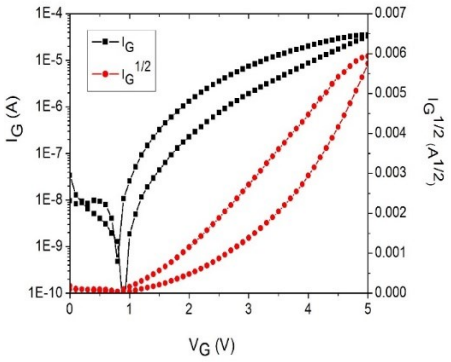
The performance of ZnO FETs with semiconductor layers annealed at 200 °C and combustion processed SA gate dielectrics deposited on ITO coated Corning glass substrate was studied. Figure 5.16 shows typical transistor characteristics of FETs with urea- based combustion processed SA dielectric operated at 5 V. The transistor exhibited a saturation field-effect mobility of 1.2 $cm^2 \cdot V^{-1} \cdot s^{-1}$, on/off current ratio of 1.1 $\times 10^4$, and subthreshold slope of 0.36 V/decade. In output characteristics, the I_D offset is defined as the I_D at different gate biases with V_D equaling zero. An I_D offset of 10 μA was observed in Figure 5.16 (a). In Figure 5.16 (c), I_G rose with the increase of potential between source and gate electrode, and reached the same order of magnitude as I_D at V_G=5 V.



(a)



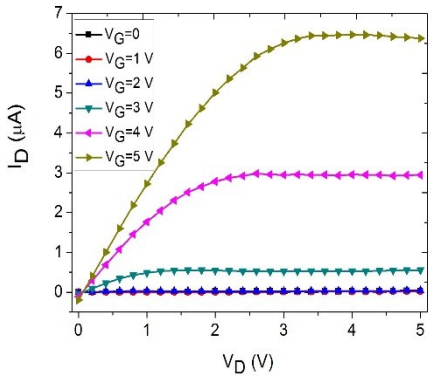
(b)



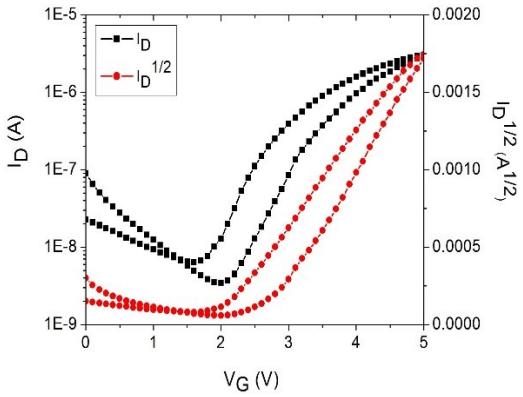
(c)

Figure 5.16 Transistor performance of ZnO FETs with urea-based combustion precursor processed SA gate dielectric. (a) Output characteristics; (b) transfer characteristics; (c) gate leakage current characteristics.

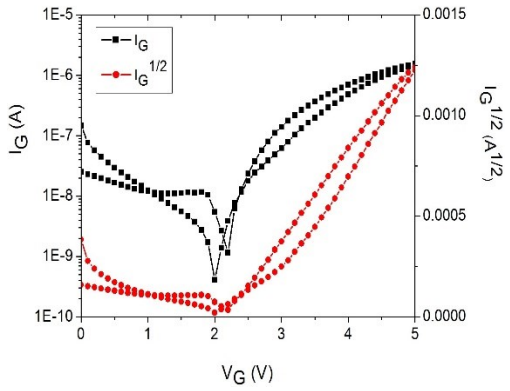
Figure 5.17 shows low temperature processed ZnO FETs with self-combustion SA gate dielectric. Compared with transistor performance shown in Figure 5.13, a smaller drain current was observed in ZnO FETs with self-combustion SA gate dielectric. This could be caused by the decrease of SA capacitance as the incorporation of GPTMS in the self-combustion precursor. In Figure 5.17 (a), I_D offset is close to zero, reflecting a small leakage current. Transistor performance parameters were calculated based on the transfer curve and shown in Table 5.2. In Figure 5.17 (c), I_G increased with the increase of V_G and finally reached the same order of magnitude as I_D.



(a)



(b)



(c)

Figure 5.17 Transistor performance of ZnO FETs with self-combustion precursor processed SA gate dielectric. (a) Output characteristics; (b) transfer characteristics; (c) gate leakage current characteristics.

To determine the ionic or electronic origin of the leakage current, a potential between a top aluminum electrode, which contacts the ZnO, and bottom ITO electrode was applied and the current through these two electrodes was measured over time. Repeating the measurement over ten times, the current between two electrodes remained at the same level rather than decreasing after a certain period of time. This suggests that the leakage current can be attributed to electron conduction rather than sodium ion conduction. Pinholes, defects, and impurities in gate dielectric films are the common reasons for high leakage current in FETs. However, considering the dense and uniform surface morphology of SA and low leakage current of SA MIM capacitors shown previously, the SA dielectric film itself may not be the main reason for high I_G observed in Figure 5.16 and Figure 5.17.

In FETs, leakage current can also originate from charge carrier tunneling due to the overlap of gate to source/drain electrodes, cross-talk between adjacent transistors, and

unfavorable expansion of source/drain electrodes within the semiconductor layer. Semiconductor patterning confines charge carriers to a desired active area and this method was widely reported to reduce gate leakage current.[24-28] Typical semiconductor patterning methods include UV light illumination, PDMS stamp patterning, photolithography, and picosecond laser patterning. In this study, the ZnO layer was patterned by a commercially available hydrophobic fluorinated polymer called Novec^{TM}. The schematic of FETs with ZnO semiconductor patterned by Novec is shown in Figure 5.18. With a patterned ZnO layer, a small I_D offset was obtained in transistor output characteristics shown in Figure 5.19 (a). At a gate-source potential of 5 V, I_G was reduced more than one order of magnitude compared with unpatterned FETs; while good FET performance was achieved with a typical saturation field-effect mobility of 0.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$, on/off current ratio of 1.02 $\times 10^3$, and subthreshold slope of 0.54 V/decade.

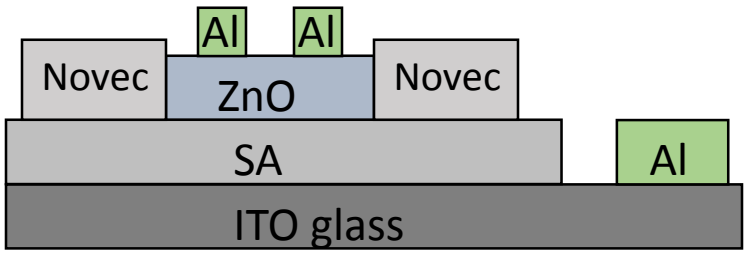
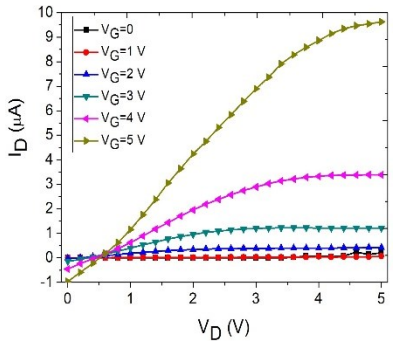
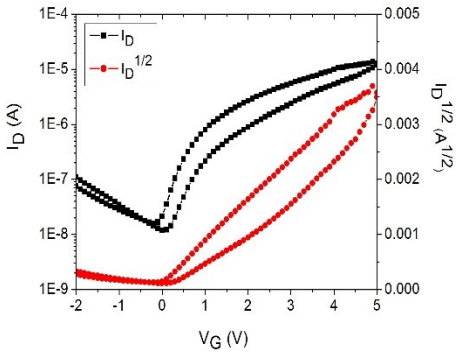


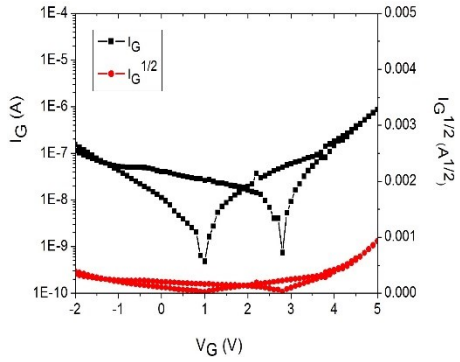
Figure 5.18 Schematics of patterned ZnO based FET configuration.



(a)



(b)



(c)

Figure 5.19 Transistor performance of ZnO FETs with self-combustion precursor processed SA gate dielectric with isolation. (a) Output characteristics; (b) transfer characteristics; (c) gate leakage current characteristics.

Table 5.2 Summary of transistor performance of low temperature processed ZnO FETs with combustion processed SA gate dielectric.

Sample	S (V/decade)	V_{th}(V)	μ_{sat} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	I_{on}/I_{off}
Urea combustion SA without patterning	0.36	2.6	1.2	1.1×10^4
Self-combustion SA without patterning	0.6	2.7	0.1	858
Self-combustion SA with patterning	0.54	1.4	0.5	1.02×10^3

5.5 Conclusions

A new aqueous ZnO sol-gel precursor for 200 °C processing was introduced with a simplified preparation procedure. With this precursor, ZnO FETs were fabricated on Si substrates with SiO_2 as gate dielectric. A typical saturation field-effect mobility of 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$, threshold voltage of 5 V, and on/off current ratio of 6.2×10^4 was obtained from these transistors. With a modified aqueous precursor, ZTO FETs were also fabricated with 200 °C and 250 °C annealing. A higher threshold voltage is observed in ZTO FETs with a saturation field-effect mobility of 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$. To reduce the operation voltage of low-temperature-processed ZnO FETs, sodium ion-incorporated alumina combustion precursors were synthesized for the first time. Two exothermic reaction peaks below 200 °C were apparent in both urea-based combustion SA precursor and self-combustion SA precursor DSC traces, reflecting low temperature precursor decomposition and film

formation. With uniform and dense thin film structure, SA MIM capacitors exhibited high capacitance and low leakage current. XRR analysis suggested an increase of SA thickness with at high GPTMS concentrations. Gate leakage current of 200 °C-fabricated all oxide FETs was likely caused by effective expansion of source/drain electrode in ZnO layers. With a ZnO layer patterned using Novec, the transistors demonstrated a significantly reduced gate leakage current and exhibited a typical saturation field-effect mobility of 0.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$, on/off current ratio of 1.02 $\times 10^3$, and subthreshold slope of 0.54 V/decade. With this, the combination of aqueous precursor processed ZnO semiconductor and SA gate dielectric demonstrates a new type of low temperature processed, low voltage operated all oxide FETs with significant potential in flexible electronics application.

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Chapter V

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Curriculum Vitae

Yu Liu was born and raised in Xiangtan, Hunan, China. He received his Bachelors of Science in Materials Science and Engineering at Nanjing University of Aeronautics and Astronautics in 2008, and Master of Science in Materials Science and Engineering at University of Florida. He joined the Materials Science and Engineering PhD program in Professor Howard Katz's group in January 2011. His research focuses on solution processing of oxide dielectric and semiconductor thin films to achieve low operation voltage and low processing temperature in low cost, large-area field-effect transistors applications. Key publications to date include:

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